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CERT. No.: 282Q19070712006



CERT. No.: 282E19070712007

# Product Specification

**Model: TOQ206XVT-01**

**2.06" AMOLED Display Module (410\*502)**

This module uses RoHS material

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## Records of Revision

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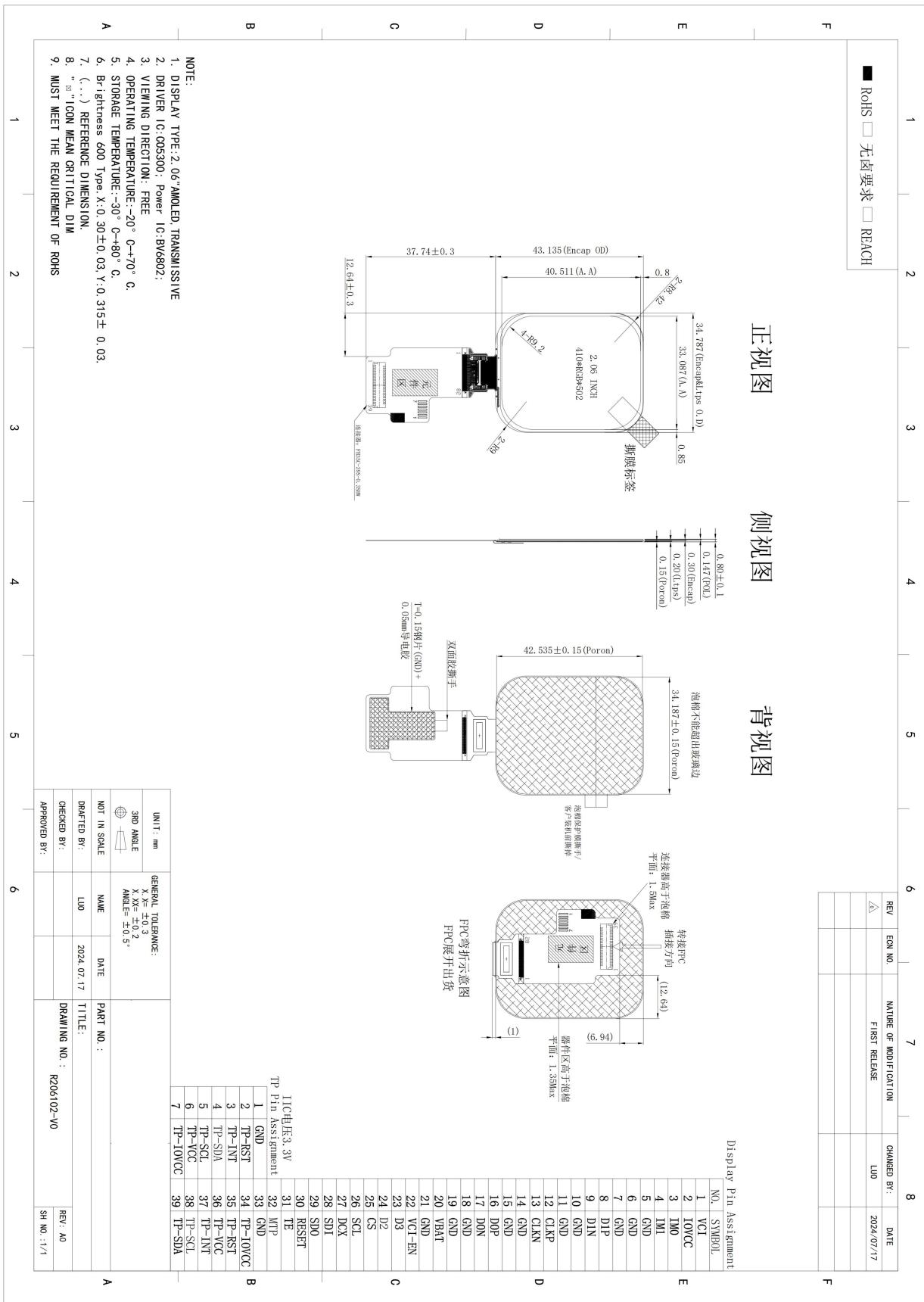
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## 1 Module Parameter

Features	Details	Unit
Display Size(Diagonal)	2.06	inch
Display Mode	AMOLED	-
Resolution	410 x 502	-
View Direction	All	Best image
Module Outline	34.787(H) ×43.135(V)×0.80(T) (Note 1 )	mm
Active Area	33.087 (H)×40.511(V)	mm
TP/CG outline	--	mm
Display Colors	16.7M	-
Interface	MIPI/QSPI/4-Wire SPI	-
Driver IC	CO5300	-
Operating Temperature	-20~70	°C
Storage Temperature	-30~80	°C
Life Time	13	Months
Weight	TBD	g

Note 1: Excluding hooks, posts , FPC/FPC tail etc.

## 2 Mechanical Drawings



### 3 Module Interface

NO	SYMBOL	FUNCTION
1	VCI	Power Supply
2	IOVCC	Power Supply for I/O System.
3	IM0	Interface type selection.
4	IM1	Interface type selection.
5	GND	Power Ground
6	GND	Power Ground
7	GND	Power Ground
8	D1P	To be ensure the trace length is shortest so that COF and FPC resistance is less than 10 Ohm.
9	D1N	To be ensure the trace length is shortest so that COF and FPC resistance is less than 10 Ohm.
10	GND	Power Ground
11	GND	Power Ground
12	CLKP	To be ensure the trace length is shortest so that COF and FPC resistance is less than 10 Ohm.
13	CLKN	To be ensure the trace length is shortest so that COF and FPC resistance is less than 10 Ohm.
14	GND	Power Ground
15	GND	Power Ground
16	D0P	To be ensure the trace length is shortest so that COF and FPC resistance is less than 10 Ohm..
17	D0N	To be ensure the trace length is shortest so that COF and FPC resistance is less than 10 Ohm.
18	GND	Power Ground
19	GND	Power Ground
20	VBAT	PMIC input power
21	GND	Power Ground
22	VCI-EN	Active high enable input pin for VCI
23	D3	8-bit bi-directional data bus for RGB I/F.
24	D2	8-bit bi-directional data bus for RGB I/F.
25	CS	Chip selection pin.Low enable.
26	SCL	This pin is used to be serial interface clock
27	DCX	D/CX = "0" : Command D/CX = "1" : Display data or Parameter
28	SDI	Serial input signal in QSPI I/F. The data is input on the rising edge of the SCL signal.
29	SDO	Serial output signal in QSPI I/F. The data is output on the rising/falling edge of the SCL signal.
30	RESET	This signal will reset the device and must be applied to properly initialize the chip.Signal is active low.pull up to avoid floating.
31	TE	Tearing effect output pin to synchronize MCU to frame writing, activated by SW command.
32	MTP	MTP programming power supply pin. (8.25V typical)
33	GND	Power Ground

34	TP-IOVCC	I/O power supply for Touch Panel
35	TP-RST	System reset of Touch Panel.
36	TP-VCC	Power Supply for Touch Panel
37	TP-INT	Interrupt signal to main processor of Touch Panel
38	TP-SCL	I <sup>2</sup> C clock signal of Touch Panel
39	TP-SDA	I <sup>2</sup> C data signal of Touch Panel.

IM[1:0]	Display Data	Command
00	MIPI / 3-wire SPI	MIPI / 3-wire SPI
01	MIPI / 4-wire SPI	MIPI / 4-wire SPI
10	MIPI / QAD-SPI	MIPI / QAD-SPI
11	MCU 8-bit	MCU 8-bit

## 4 Absolute Maximum Ratings

Maximum Ratings (Voltage Referenced to VSS) VSS=0V, Ta=25°C

Item	Symbol	Min.	Max.	Unit
Analog Supply Voltage	Display IC	VCI	-0.3	+5.5
Logic Supply Voltage	Display IC	IOVDD	-0.3	+5.5
Positive Power Input	Power IC	ELVDD	-	+6.6
Negative Power Input	Power IC	ELVSS	-5.0	-

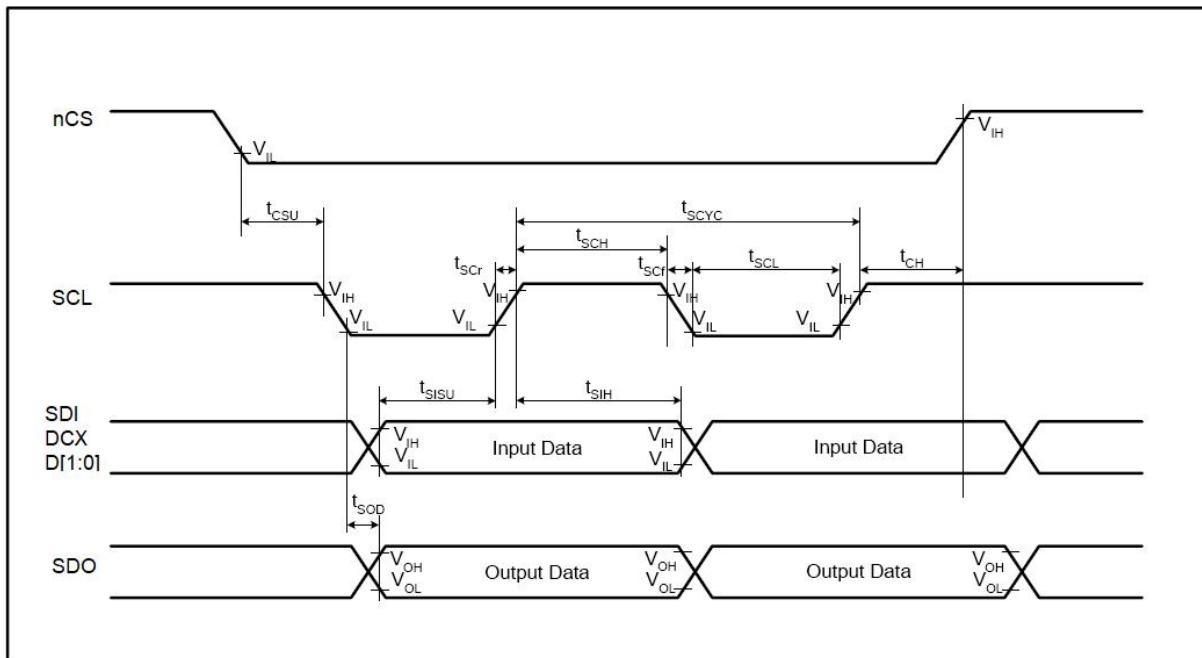
## 5 DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Analog Supply Voltage	VCI	2.5	2.8	3.3	V
Logic Supply Voltage	IOVDD	1.65	1.8/2.8	3.3	V
Positive Output Voltage	ELVDD	-	3.3 @ Normal/AOD	3.5 @HBM	V
Negative Output Voltage	ELVSS	-3.5 @HBM	-3.3 @ Normal/AOD	-	
Logic Low input voltage	V <sub>IL</sub>	VSS	-	0.3IOVC C	V
Logic High input voltage	V <sub>IH</sub>	0.7IOVCC	-	IOVCC	V
Logic Low output voltage	V <sub>OL</sub>	VSS	-	0.2IOVCC	V
Logic High output voltage	V <sub>OH</sub>	0.8IOVCC	-	IOVCC	V
Power Consumption Of display (Note1)	Normal mode	-	239.15	-	mW
	Standby mode	-	0.68	-	mW
	HBM mode	-	443.9	-	mW
Frame Frequency	f <sub>FR</sub>	-	60	-	Hz

Note 1: Power Supply : DDIC CO5300 VCI=3.3V, VDDIO=1.8V, ELVDD=3.3V , ELVSS=-3.3V

## 6 AC Characteristics

### 6-1 Serial Interface Characteristics (QUAN SPI)



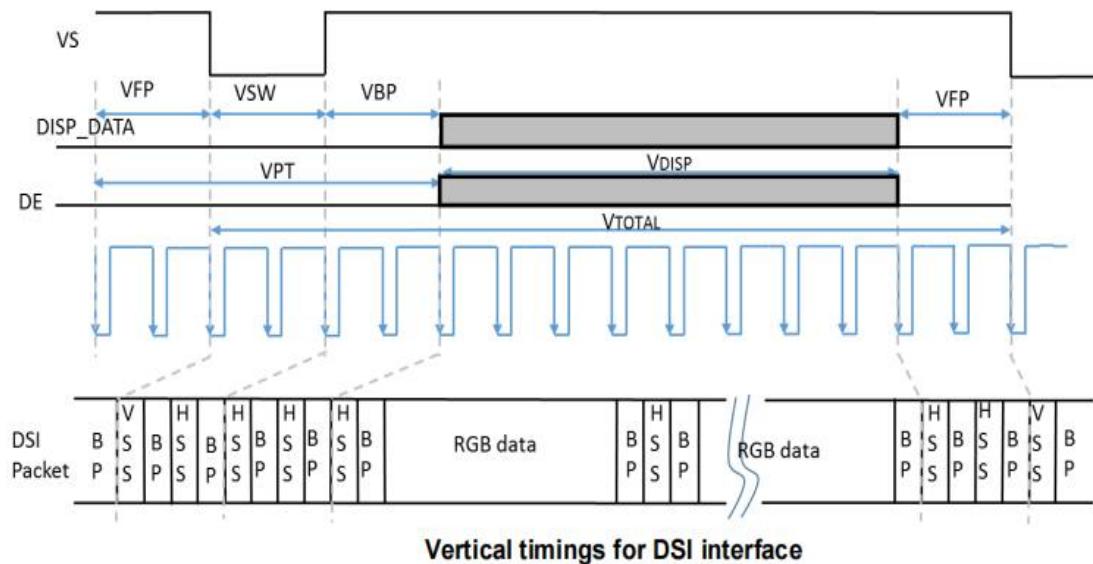
Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
SCL	$T_{SCYC}$	Clock cycle (Write)	20	-	-	ns	
	$T_{SCYC}$	Clock cycle (Read)	100	-	-	ns	
	$T_{SCH}$	Clock "H" pulse width (Write)	6.5	-	-	ns	
	$T_{SCH}$	Clock "H" pulse width (Read)	45	-	-	ns	
	$T_{SCL}$	Clock "L" pulse width (Write)	6.5	-	-	ns	
	$T_{SCL}$	Clock "L" pulse width (Read)	45	-	-	ns	
	$T_{SCR}$	Clock rise time	-	-	3.5	ns	
	$T_{SCR}$	Clock fall time	-	-	3.5	ns	
CSX	$T_{CSU}$	Chip select setup time	10	-	-	ns	
	$T_{CH}$	Chip select hold time	10	-	-	ns	
SDI DCX D[1:0]	$T_{SISU}$	Data input setup time	4	-	-	ns	
	$T_{SIH}$	Data input hold time	4	-	-	ns	
SDO	$T_{SOD}$	Data output setup time	-	-	45	ns	
	$T_{SOH}$	Data output hold time	5	-	-	ns	

**Note 1:** Logic high and low levels are specified as 20% and 80% of VDDI for Input signals.

**Note 2:**  $T_a = -30$  to  $85$  °C,  $VDDI=1.65V$  to  $3.3V$ ,  $VCI=2.7V$  to  $3.6V$ ,  $GND=0V$

**Note 3:** The max SCL sequence of 4-wire QSPI transferring RGB888, RGB666 and RGB555 is 50Mhz.

## 6.2 Vertical timings for DSI video mode



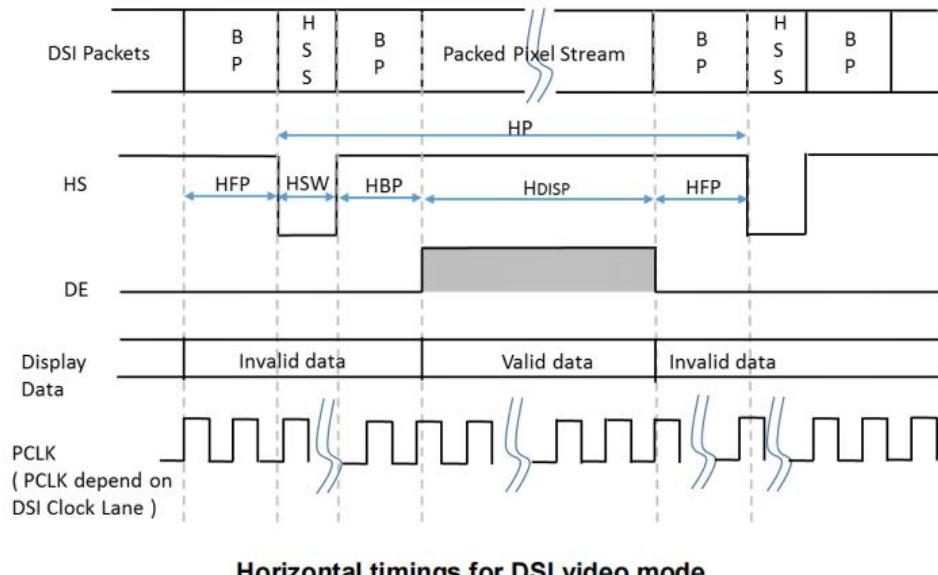
Condition :  $T_a = 25^\circ\text{C}$ , Resolution = 454(RGB) \* 454

Vertical Timings List for DSI video mode

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Vertical Total	VTOTAL			TBD		Line	
Vertical low pulse width	VSW			TBD		Line	1
Vertical front porch	VFP			TBD		Line	
Vertical back porch	VBP			TBD		Line	1
Vertical data start point		VSW+VBP		TBD		Line	1
Vertical blanking period	VPT	VSW+VBP+VFP		TBD		Line	
Vertical active area	VDISP			454		Line	
Vertical Frame rate	VFR			60		Hz	

*Note 1: The VSW and VBP pulse width are related to GOA timing. The GOA timing must be set at corresponding position for*

### 6.3 Horizontal timings for DSI video mode



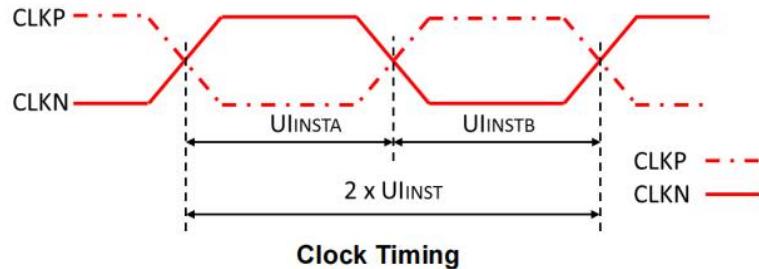
Condition :  $T_a = 25^\circ\text{C}$ , Resolution = 454(RGB)\* 454

Horizontal Timings List for DSI video mode

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
HS low pulse width	HSW			TBD		nS	
Horizontal back porch	HBP			TBD		nS	
Horizontal front porch	HFP			TBD		nS	
Horizontal data start point		HSW+HBP		TBD		nS	
Horizontal blanking period	HBLK	HSW+HBP+HFP		TBD		nS	
Horizontal active area	HDISP			454		DCLK	

## 6.4 MIPI AC Characteristics

### 6.4.1 High speed mode - clock timings

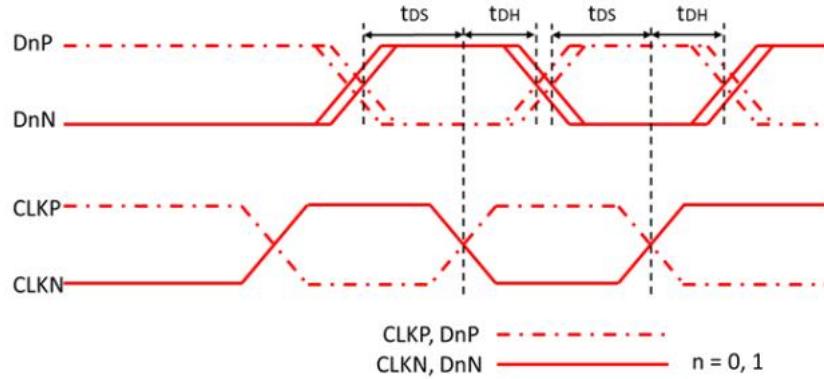


High Speed Mode - Clock Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
CLK P/N	$2 \times UI_{INST}$	Double UI instantaneous	4		25	nS	
CLK P/N	$UI_{INSTA}, UI_{INSTB}$	UI instantaneous Half	2		12.5	nS	1

**Note 1:**  $UI = UI_{INSTA} = UI_{INSTB}$ .

### 6.4.2 High speed mode - clock /data timings



DSI Clock / Data Timings

High Speed Mode - Clock / Data Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
Dn P/N (n=0, and1 )	$t_{DS}$	Data to Clock Setup time	0.15*UI			UI	
	$t_{DH}$	Clock to Data Hold time	0.15*UI			UI	

### 6.4.3 High speed mode - rising and falling timings

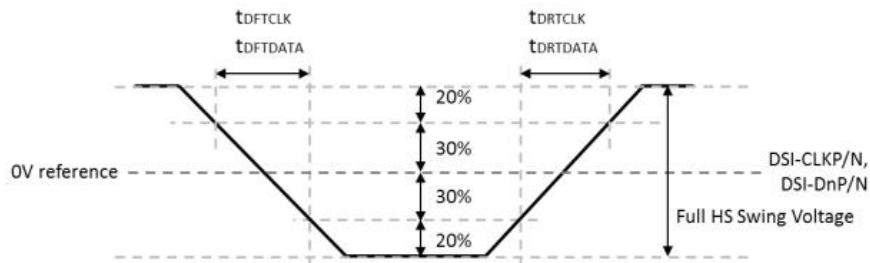


Figure 6-2 Rising and Falling Timings

High Speed Mode - Rising and Falling Timing

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Differential Rise Time for Clock	$t_{DRCLK}$	CLKP/N	150pS		0.3*UI		2,3
Differential Rise Time for Data	$t_{DRDATA}$	DnP/N	150pS		0.3*UI		1,2,3
Differential Fall Time for Clock	$t_{DFTCLK}$	CLKP/N	150pS		0.3*UI		2,3
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N	150pS		0.3*UI		1,2,3

**Note 1:**  $DnP/N$ ,  $n = 0$ , and 1.

**Note 2:** The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-PHY standard.

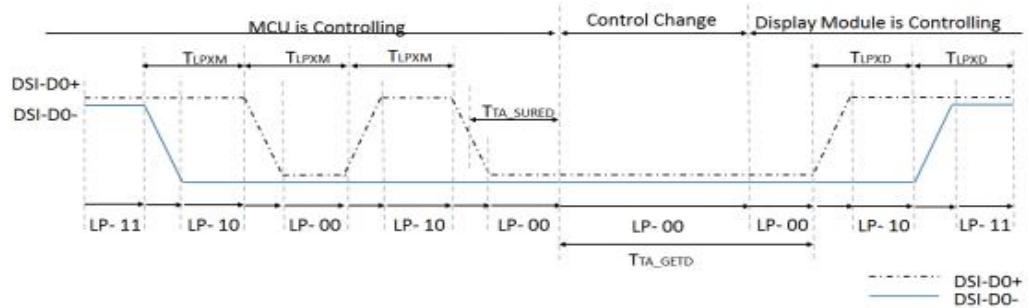
**Note 3:**  $DSI-CLK+ = CLKP$ .

$DSI-CLK- = CLKN$ .

$DSI-D0+ = D0P$ .

$DSI-D0- = D0N$ .

#### 6.4.4 Low speed mode - bus turn around



Bus Turnaround (BTA) from MCU to display module Timing

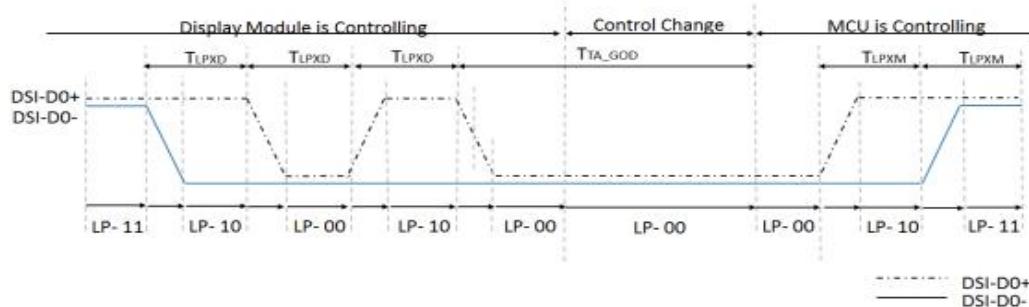


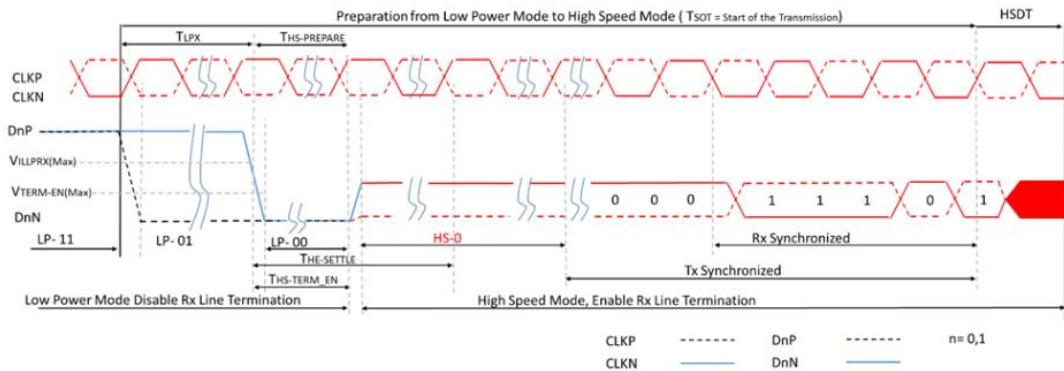
Figure 6-3 Bus Turnaround (BTA) from Display module to MCU Timing

Low Speed Mode - Bus Turn Around Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
D0P/N	TLPXM	Length of LP-00,LP-01,LP-10 or LP11 periods MCU to Display Module	50		75	nS	1
D0P/N	TLPXD	Length of LP-00,LP-01,LP-10 or LP11 periods Display Module to MCU	50		75	nS	1
D0P/N	TTA_SURED	Time-out before the Display Module starts driving	TLPXD		2* TLPXD	nS	1
D0P/N	TTA_GETD	Time to drive LP-00 by Display Module	5* TLPXD			nS	1
D0P/N	TTA_GOD	Time to drive LP-00 after turnaround request -MCU	4 * TLPXD			nS	1

Note 1: D0P = DSI-D0+, D0N = DSI-D0-.

### 6.4.5 Data lanes from low power mode to high speed mode



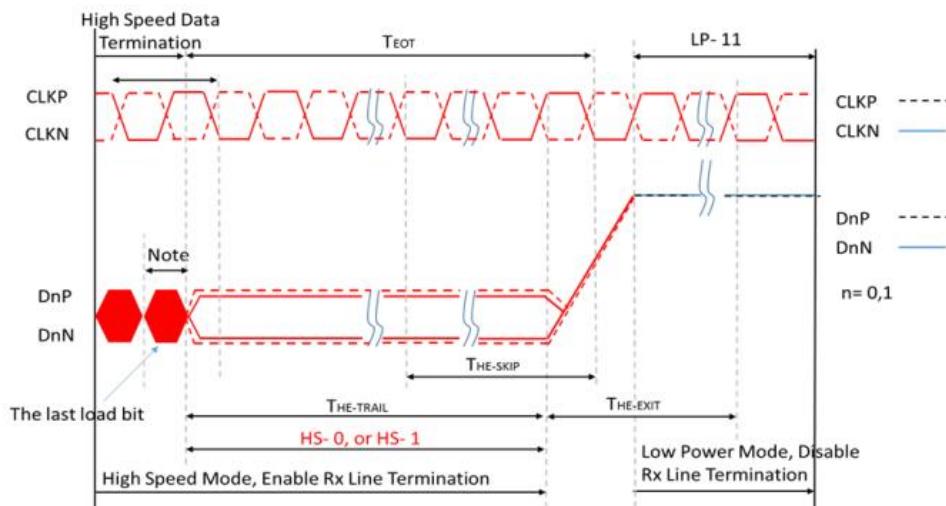
**Data Lanes from High Speed Mode to Low Power Mode Timing**

**Data Lanes from Low Power Mode to High Speed Mode Timing**

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
DnP/N	T <sub>LPX</sub>	Length of any Low Power State Period	50			nS	1
DnP/N	T <sub>HS-PREPARE</sub>	Time to drive LP-00 to prepare for HS Transmission	40+4*UI		85+6*UI	nS	1
DnP/N	T <sub>HS-TREM-EN</sub>	Time to enable Data lane Receiver line termination measured from when Dn crosses VILMAX			35+4*UI	nS	1

**Note 1:** DnP/N, n=0, and 1

#### 6.4.6 Data lanes from high speed mode to low power mode



*Note:*  
If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.  
If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0

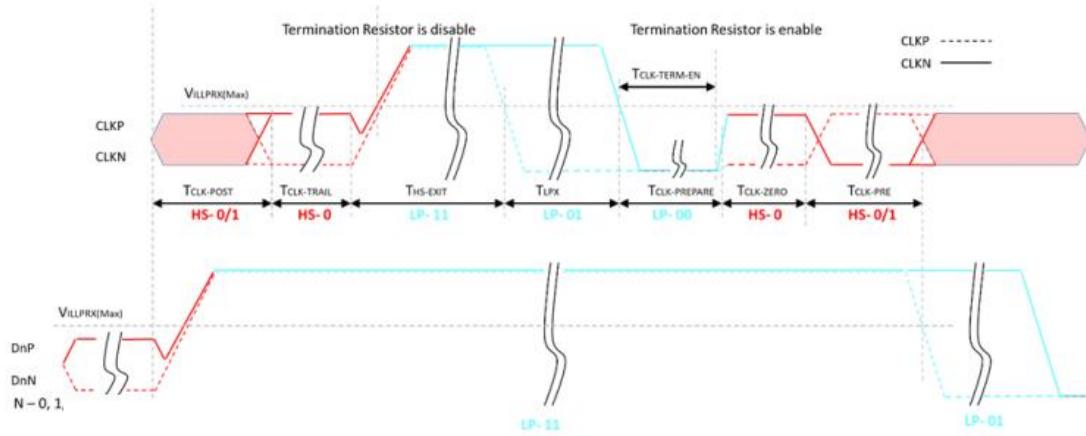
#### Data Lanes from High Speed Mode to Low Power Mode Timing

##### Data Lanes from High Speed Mode to Low Power Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
DnP/N	T <sub>HS-SKIP</sub>	Time-Out at Display Module to ignore transition period of EoT	40		55+4*UI	nS	1
DnP/N	T <sub>HS-EXIT</sub>	Time to drive LP-11 after HS burst	100			nS	1

**Note 1:** DnP/N, n=0, and 1.

#### 6.4.7 DSI clock burst - high speed mode to/from low power mode

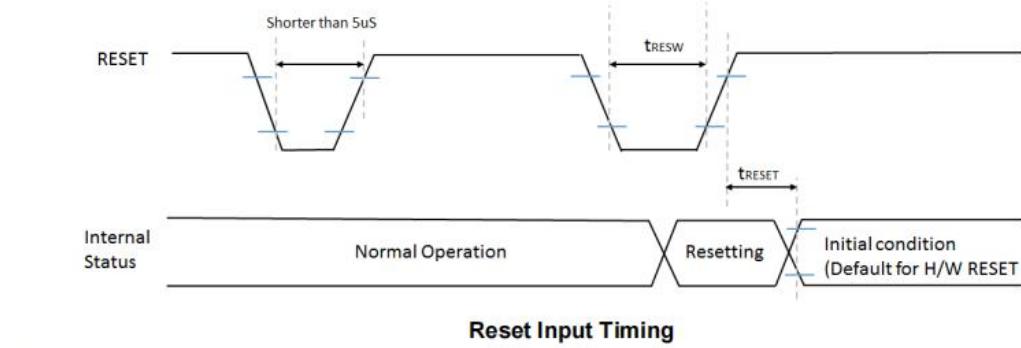


**Clock Lane –High speed mode to / from Low Power Mode Timing**

**DSI Clock Burst – High speed mode to /from Low Power Mode Timing**

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
CKP/N	TCLK-POST	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52*UI			nS	
CKP/N	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60			nS	
CKP/N	THS-EXIT	Time to drive LP-11 after HS burst	100			nS	
CKP/N	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38		95	nS	
CKP/N	TCLK-TERM-EN	Time-out at Clock Lane to enable HS termination			38	nS	
CKP/N	TCLK-PREPARE+ TCLK-ZERO	Minimum lead HS-0 drive period before starting Clock	300			nS	
CKP/N	TCLK-PRE	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8*UI			nS	

## 6.5 Reset input timing



**Reset Input Timing**

Signal	Symbol	Parameter	Description	Specification			Unit	Notes
				MIN	TYP	MAX		
RESET	$t_{RESETW}$	Reset "L" pulse width		10			$\mu\text{S}$	1
	$t_{RESET}$	Reset complete time	When reset applied during Sleep in mode			5	$\text{mS}$	2
			When reset applied during Sleep Out mode			120	$\text{mS}$	5

**Note 1:** Spike due to an electrostatic discharge on RESET line does not cause irregular system reset according to the table below.

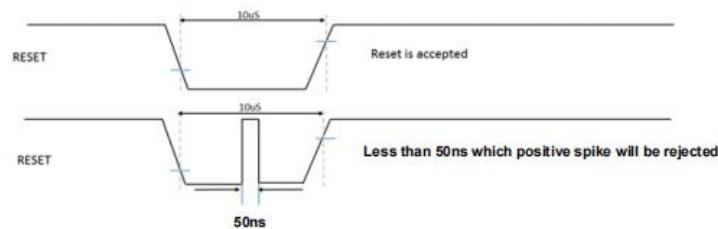
**Reset Input Actions**

RESET Pulse	Action
Short than 5us	Reset Rejected
Long than 10 $\mu\text{S}$	Reset
Between 5us and 10 $\mu\text{S}$	Reset Start

**Note 2:** During the resetting period, the display will be blanked ( The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in sleep out mode. The display remains the blank state in sleep in mode) and then return to Default condition for H/W RESET.

**Note3:** During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W RESET complete time( $t_{RESET}$ ) within 5ms after a rising edge of RESET.

**Note4:** Spike Rejection also applies during a valid reset pulse as shown below.



**Note5:** It is necessary to wait 5ms after releasing RESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

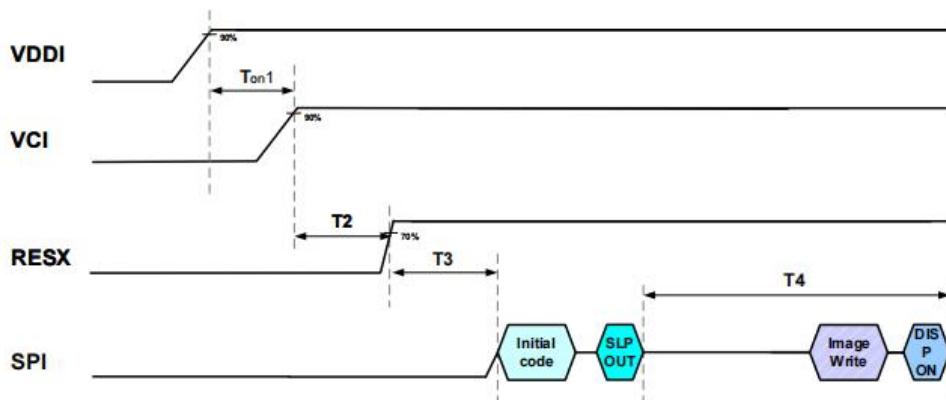
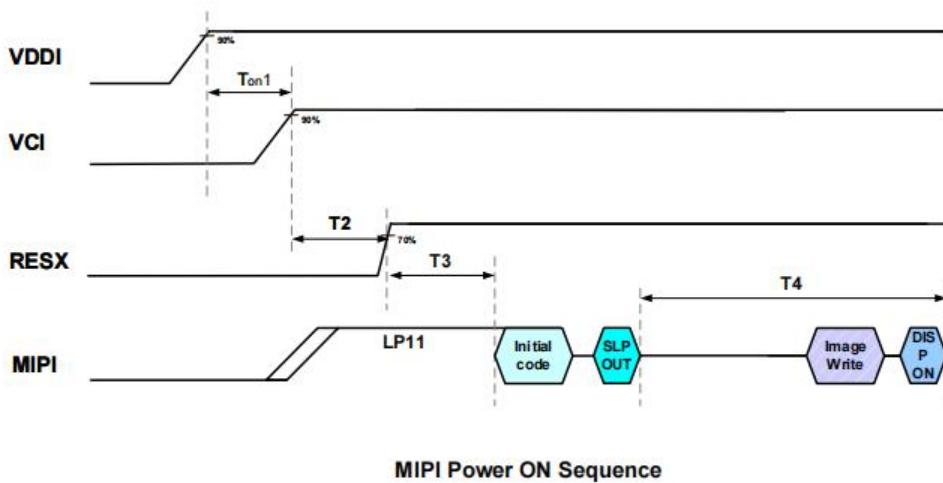
## 6.6 Power on sequence

The power on sequence for different power input modes are shown below figures.

Power ON Sequence Timing

Symbol	Description	Value			Unit	Remark
		Min.	Typ.	Max.		
Ton1	VDDI on to VCI on delay	>0			us	
T2	VDDI on to valid to RESET high	10			ms	
T3	RESET high to first command	10			ms	
T4	Sleep-out command received to Display on command received.	60			ms	

The Power on sequence is shown as below.



**Note 1:** Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

**Note 2:** This power-on sequence is based on adding Schottky diode on VGL pin to ground.

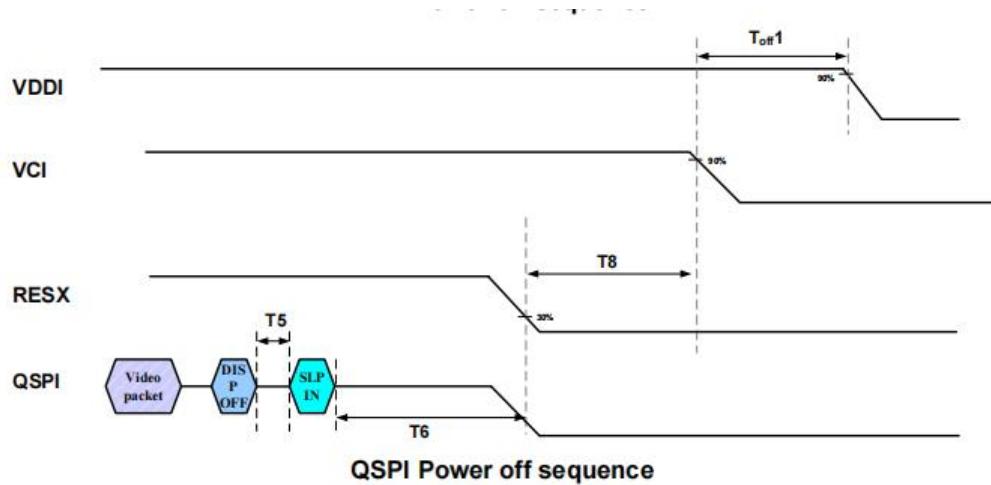
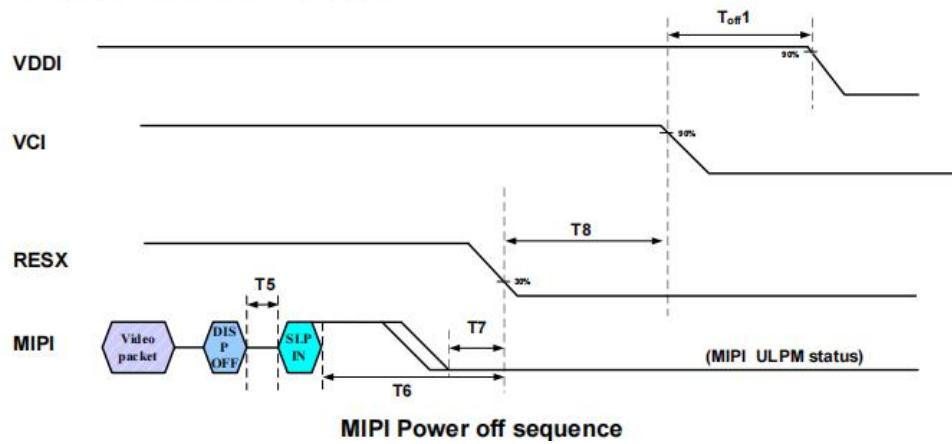
## 6.7 Power off sequence

The power off sequence for different power input modes are shown below figures.

Power OFF Sequence Timing

Symbol	Description	Value			Unit	Remark
		Min.	Typ.	Max.		
T <sub>off1</sub>	VCI off to VDDI off delay	>0			us	
T <sub>5</sub>	Display-off command received to Sleep-in command delay	>0			us	
T <sub>6</sub>	Sleep-in command received to valid to RESET low	83			ms	@60Hz
T <sub>7</sub>	MIPI ultra low power mode to valid to RESET low	0			us	
T <sub>8</sub>	RESET low to VCI off delay	0			us	

The power off sequence is shown as below:



**Note 1:** Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

**Note 2:** Keep VGH is equal to or larger than VCI during power off sequence.

## 7 Optical Specifications

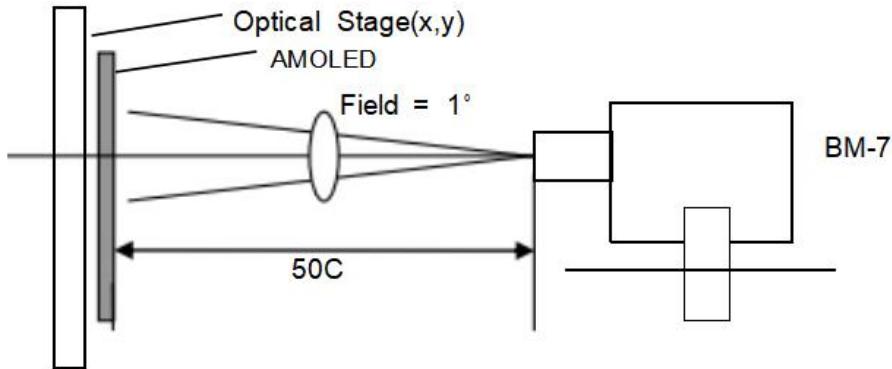
Test condition : VDDIO=1.8V , VCI=3.3 V, Ta=25°C

Item	Symbol	Condition	Value			Unit	Note	
			Min	Typ	Max			
Luminance	Bp		540	600	-	nit		
Uniformity	△Bp	W255	85	-	-	%	Note 5	
Viewing Angle	Left	θL	CR≥10	80	85	-	Degree	Note 2
	Right	θR		80	85	-		
	Top	ψT		80	85	-		
	Bottom	ψB		80	85	-		
Contrast Ratio	Cr	Θ=0°	60000:1	-	-	-	Note 3	
Color Coordinate of CIE1931 (with lens)	Red	X		0.642	0.682	0.722	-	
		Y		0.275	0.315	0.355		
	Green	X		0.190	0.240	0.290		
		Y		0.660	0.710	0.760		
	Blue	X		0.100	0.140	0.180		
		Y		0.008	0.048	0.088		
	White	X		0.280	0.300	0.320		
		Y		0.295	0.315	0.335		
NTSC Ratio	NTSC		97	100	-	%	Note 4	
Lifetime	LT95	At 25°C, with white color pattern	200	-	-	h	Normal mode	

### Definition of Response Time

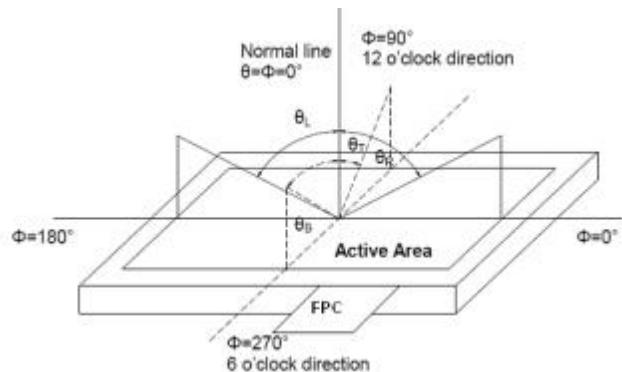
- 1.the ambient temperature is 25°C .
- 2.The test systems refer to Note1 and Note2.

### Note 1: Definition of optical measurement system.



### Optical Characteristic Measurement Equipment and Method

### Note 2: Definition of viewing angle range and measurement system.



### Note 3: Definition of contrast ratio

$$\text{Contrast ratio(CR)} = \frac{\text{Luminance measured when AMOLED is on the "white" state}}{\text{Luminance measured when AMOLED is on the "Black" state}}$$

"White state": A state where the AMOLED should be driven by V white.

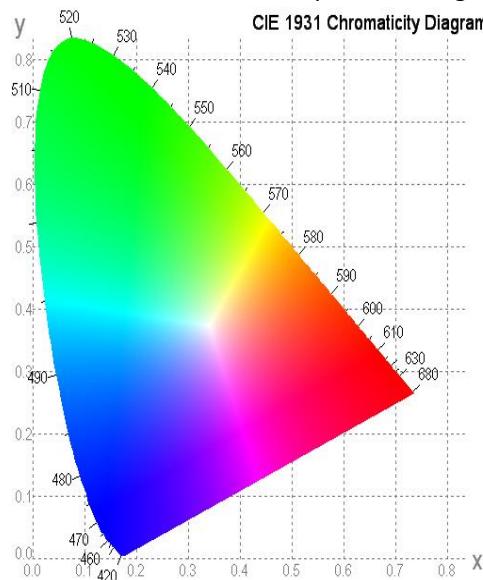
"Black state": A state where the AMOLED should be driven by V black.

**Note 4: Definition of color chromaticity (CIE1931)**

R,G,B and W are defined by (x, y) on the IE chromaticity diagram

NTSC=area of RGB triangle/area of NTSC triangleX100%

Measuring picture: Red, Green, Blue and White (Measuring machine: BM-7)

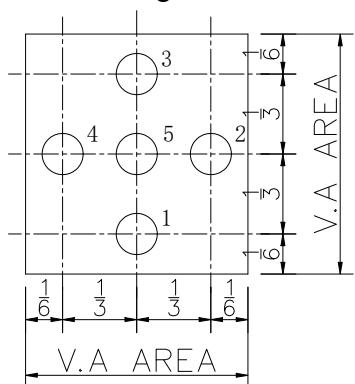
**Note 5: Definition of luminance uniformity**

Using the transmissive mode measurement approach, measure the white screen luminance of the display panel and backlight.

Surface Luminance: LV = average (LP1:LP5)

Uniformity = Minimal (LP1:LP5) / Maximal (LP1:LP5) \* 100%

Note :Measuring machine:BM-7



## 8 Quality Assurance

### 8.1 AMOLED Module of Characteristic Inspection

The environmental condition and visual inspection shall be conducted as below:

8.1.1 Test conditions: OLED is not light, cold white fluorescent lamp, illumination  $1000 \pm 200$ lux; OLED lighting source shall not be higher than 200lux, with black background around.

8.1.2 Inspection distance: the standard observation distance of all surfaces of the tested object is  $30\text{cm} \pm 5\text{cm}$ .

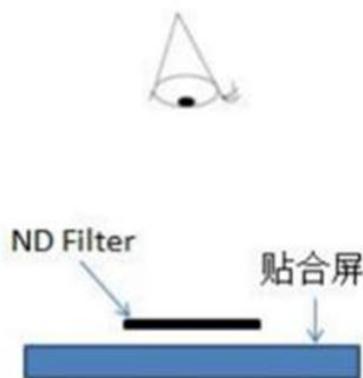
8.1.3 Inspection angle: the angle between the product and the horizontal plane is  $45^\circ$ , and the eyes are perpendicular to the inspection plane. During inspection, the product needs to rotate  $45^\circ$  up, down, left and right. The observation line of sight needs to be within the half section of the cone. The observation angle is  $45^\circ$  with the vertical axis of the product apex. The central axis of the cone must be standard and perpendicular to the product surface and pass through the fluorescent lamp; For non- conventional display defects (including but not limited to local bright lines or local floodlights), the observation angle is 75 degrees from the normal of the product surface; Full visual angle of appearance.

8.1.4 Inspection time: the inspection time without lighting is at least 10-12 seconds; The time of OLED lighting inspection for each picture is 1~3 seconds. If the defect is still not visible within the specified time, the inspection piece is deemed to be qualified.

8.1.5 Test temperature: room temperature  $15-35^\circ\text{C}$ , ambient humidity: 20-75% RH.

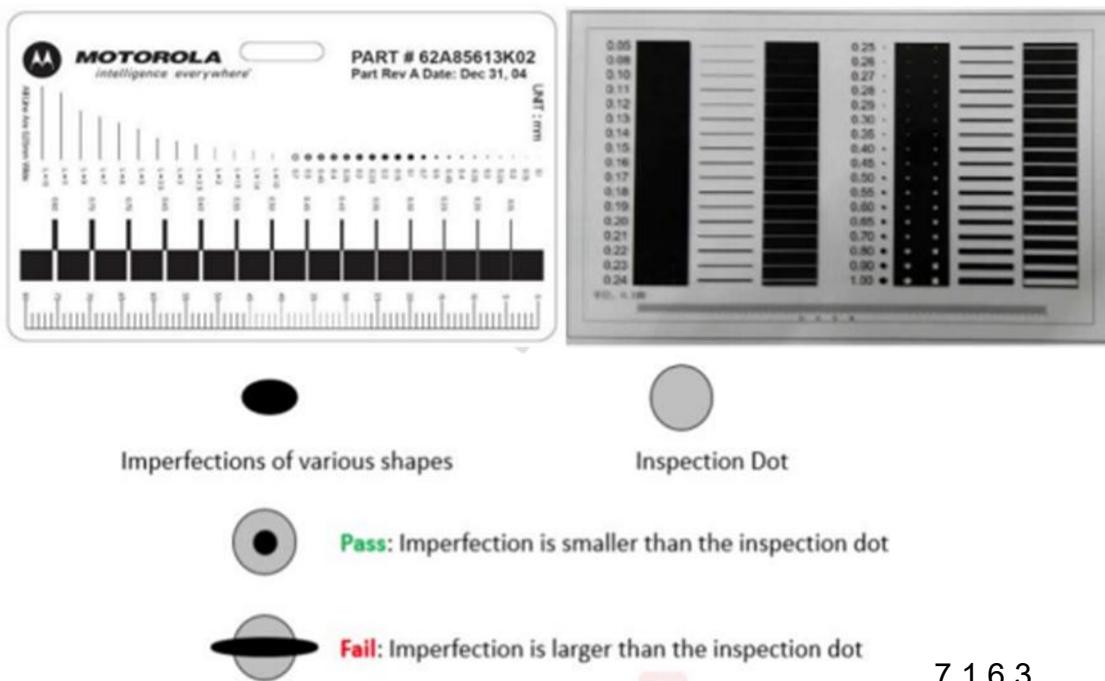
8.1.6 Inspection tools:

8.1.6.1 ND Filter: The ND Filter is placed at a distance of 2-3 cm above the defect for 2-3s to judge whether the defect is visible. As Figure below: (ND Filter is used to test mura isochromatic and light unevenness)



8.1.6.2 Point gauge (point gauge in the figure below is recommended), determination method: as shown in the figure, the point gauge film can cover is pass, and the point gauge film can not cover

is Fail. For example, a maximum of 0.2mm same-color spot defect is allowed on the Class A surface, and the pass that can be covered by 0.2mm on the film, The one that can be covered is Fail.



### 7.1.6.3

Microscopic examination: use 20-50 times adjustable microscope and 10-30 times test eyepiece.

8.1.6.4 Digital caliper: resolution 0.01mm.

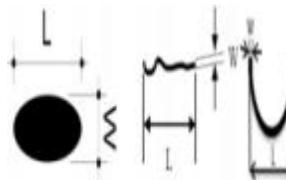
8.1.6.5 Projector: anime microscope, 3D projector.

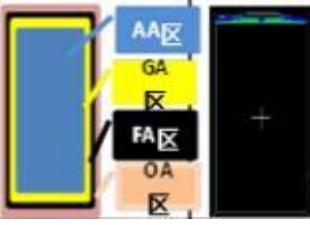
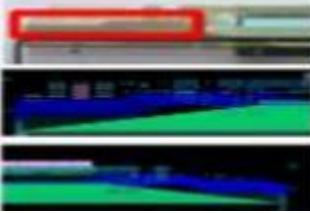
8.1.6.6 Judgment description

8.1.6.6.1 The measurement accuracy shall refer to the specification definition. When the measurement equipment accuracy is higher than the specification definition, the measured value needs to be rounded to the precision defined by the specification. For example, the size of edge collapse is 0.20mm, and the thousandth is the reference position, which is rounded to 0.200mm~0.204mm is OK,  $\geq 0.205\text{mm}$ , it is judged as NG.

8.1.6.6.2 In addition to the tools used above, if additional inspection tools are needed to assist the judgment, they can only be carried out after the coordination of both parties.

8.1.6.6.3 Bad code and definition

Code and name		legend	explain
N	Number	-	Visually calculate the number; The statistics of the total number of defects does not include the completely "omitted" part. For the column defined as "omitted" and "omitted", it is not counted as the number of defects if it meets the requirements, otherwise it is calculated as an independent defect.
L	Length (mm)		Dot line distinguishing rule: L is the long side, W is the short side A. When $L > 3W$ , handle as per line, otherwise handle as per point;
W	Width (mm)		B. When it is judged as line defect, S-shaped or C-shaped line appears, and the enclosed amount is less than 3/4 circle, it shall be treated as line defect; otherwise, it shall be treated as point defect, and the inner tangent circle shall simulate the size of point.
S	Area ( $\text{mm}^2$ )	-	Surface gauge
D	Diameter (mm) $D=(L+W)/2$	-	Point diameter calculation: calculated by half of the sum of the long side and the short side, that is,

			D=(L+W)/2, where D represents the diameter of the point, L is the long side, and W is the short side;
H	Depth (mm)	-	Digital micrometer
DS	Distance (mm)		Distance between two points or between two lines
Schematic diagram of screen area			AA area: display area; GA area: GIP circuit area; FA area: Frit area; OA area: outside FA area
Leader area			Screen GIP circuit area, screen data circuit area
PAD Bonding District			COG/FOG Bonding alignment mark and Bonding Pad on LTPS substrate
PAD Non-stat e area			Screen test pad, cutting area and lead-free area on LTPS substrate
CT crimping area			Pin end screen test pad

Highlights		A single sub-pixel (or red, or green, or blue) of one pixel is called a point; The definition of bright spot is that in the environment of $200 \pm 50$ Lux, the pixels or dots seen by employees with naked eyes are always bright, and the bright spot is checked under the black screen
Scotoma		A single sub-pixel (or red, or green, or blue) of one pixel is called a point; A dark point is defined as a point that is not bright in a single sub-pixel seen with naked eyes in a 100% white picture under the environment of $200 \pm 50$ Lux.
Dark spot - two connection		Two adjacent sub-pixels under the magnifying glass are not bright at the same time (horizontal, vertical and oblique)
Dark Spot - Three Links		The adjacent R, G and B sub-pixels under the magnifying glass are not bright at the same time (horizontal, vertical and oblique)
CG monomer area division		AA: Front visible area, black ink internal area; A: Black ink area; B: Cover plate edge; The front defect that runs through the AA area and the A area shall be judged according to the specification of the strictest area, and the back defect shall be judged according to whether the AA area is visible.
Foreign matter highlights	-	Due to the foreign matter in the polarizer, the phenomenon that appears as a bright spot is called a foreign matter bright spot

point defect		<p>There are bright spots and black spots in local positions, including but not limited to the internal dirt of the screen itself, pinholes, serrations, concave-convex spots, color spots, tiny bubbles, white spots, stains on the fitting of the polarizer, poor polarizer itself and other spot-like defects. Point defects are judged by diameter.</p>
Linear defect		<p>Linear impurities in the screen, including filaments, fibers, polarizer fitting impurities in the screen, and scratches on the surface of polarizer, etc. Linear defects are judged by length and width.</p> <p>Sensible scratch: also known as hard scratch, is a deep scratch on the surface, which is felt by hand.  Senseless scratch: also known as fine scratch, no deep scratch on the surface, no feeling when touching.</p>
Serrated defect		<p>W: Distance from sawtooth crest to trough</p>
Edge collapse/angle collapse		<p>In the process of screen production, especially in the process of molding and cutting, the small glass missing at the glass edge is caused.</p> <p>X direction: parallel to FOG Pad or glass edge;  Y direction: perpendicular to FOG Pad or glass edge;  Z direction: screen thickness direction;</p>
Pitting	-	<p>In the unit area of 10mm * 10mm, the defect point with <math>D \leq 0.1\text{mm}</math>, <math>DS \geq 2\text{mm}</math>, and the number <math>N \geq 5</math>. If the customer has other requirements, follow the customer's requirements.</p>
Dirty	-	<p>Including handprints, oil stains, fingerprints, stains, white fog and other undesirable phenomena. It is divided into erasable dirt and non-erasable dirt.</p>

		<p>Use a dust-free cloth dipped in alcohol, which can not be erased as non-erasable dirt. Wipable dirt is determined as follows:</p> <p>A. Dry dust-free cloth can be directly erased;</p> <p>B. Wipe with clean cloth dipped with anhydrous alcohol</p> <p>Press the alcohol-stained dust-free cloth on the dry dust-free cloth twice to absorb excess alcohol; Wipe back and forth with a dust-free cloth twice, and the dirt can be removed.</p>
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## 8.2 Sampling Procedures for Each Item Acceptance Table

Critical Defect (CR): any defect that directly or indirectly affects human health and safety, or the function of the product is lost.

Major Defect (MA): directly or indirectly affect the product function, or make part of the product function lost, and other customers do not acceptable defects.

Minor Defect (MI): appearance defect that does not affect product function and can be accepted by customers.

Defect Type	Sampling Procedures	AQL
Major Defect (MA)	Take the normal inspection solution of the sampling plan of GB/T2828.1-2012 Inspection level II	0.6
Minor Defect (MI)	Take the normal inspection solution of the sampling plan of GB/T2828.1-2012 Inspection level II	1

## 8.3 Telecommunication inspection standard

category	NO.	Inspection items	Inspection specification	test mode	defect type
Poor function	1	Display exception	not allow	visual	CR
	2	No display	not allow	visual	CR
	3	The picture flickers	not allow	visual	MA

TP function	4	TP test NG	not allow	visual	MA
Dot	5	Bright dot	not allow Remark : Using the Visionox T-aging condition	visual	MI
	6	Partial Bright dot	ND6% or reference limit sample Remark : Using the Visionox T-aging condition	visual	MI
	7	Dark dot	1.D≤0.15mm, ignored; 2.0.15mm < D≤ 0.2mm, DS ≥ 10mm, N ≤ 10; 3.D > 0.2mm,not allowed;	Visual inspection, Flinka	MI
Line	8	Bright line	not allow	visual	MA
	9	Dark line	not allow	visual	MA
	10	Slightly bright line	not allow	visual	MA
Mura	11	horizontal mura	No control under W64/128 screen; The 4%ND Filter on the 255 screen determines that the invisible is OK and the visible is NG.	Visual ND Filter/limit sample	MI
	12	vertical mura	No control under W64/128screen; The 4% ND Filter on the 255 screen determines that the invisible is OK and the visible is NG.	Visual ND Filter/limit sample	MI
	13	White spot	No control under W64/128 screen; The 4% ND Filter on the 255 screen determines that the invisible is OK and the visible is NG.	Visual ND Filter/limit sample	MI
	14	Black spot	No control under W64/128 screen; The 4% ND Filter on the 255 screen determines that the invisible is OK and the visible is NG.	Visual ND Filter/limit sample	MI

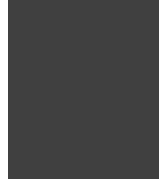
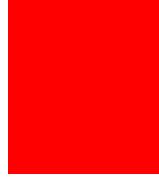
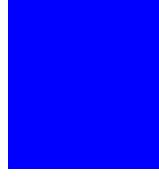
	15	Color mura	4% ND Filter in W64/255 screen determines that the invisible is OK and the visible is NG	Visual ND Filter/limit sample	MI
	16	snowflake	No control under W64/128 screen; The 4% ND Filter on the 255 screen determines that the invisible is OK and the visible is NG.	Visual ND Filter/limit sample	MI
	17	Twill mura	No control under W64/128 screen; The 4% ND Filter on the 255 screen determines that the invisible is OK and the visible is NG.	Visual ND Filter/limit sample	MI
	18	Newtonian ring	No control under W64/128 screen; The 4% ND Filter on the 255 screen determines that the invisible is OK and the visible is NG.	Visual ND Filter/limit sample	MI
	19	Uneven transition	Reference homogeneity standard to assist in judgment; The 4% ND Filter in the W64/255 screen determines that the invisible product is OK and the visible product is NG.	Visual ND Filter/limit sample	MI
	<p>1、Mura all specify the screen judgment. For example, if the ELA mura judgment standard is 255, the ELAmura will only be judged on the W255 screen.</p> <p>2、Other types of mura have a low adverse effect rate and low incidence. According to the 4% ND Filter in the W64/255 screen, the invisible products are OK and the visible ones are NG.</p>				
Dot/line of foreign material	20	Dot/line defects (foreign material, black white dot, scratch, bubble, etc.)	Same as other views/specifications of linear defects	Visual inspection/Flinka	MI

#### 8.4 Appearance inspection standard

NO.	Inspection items	Inspection specification	test mode	defect type
1	Broken glass	not allow	visual	MA
2	crack	not allow	visual	MA
3	Edge collapse/corner	1. $Y \leq 0.15\text{mm}$ , X and N are ignored; 2. $0.15 < Y \leq 0.4\text{mm}$ , $X \leq 2\text{mm}$ , N is ignored;	Visual inspection, Flinka	MI

		3. $Y > 0.4\text{mm}$ , not allowed; 4. $Z \leq t$ ;		
4	flange	1. $Y \leq 0.2\text{mm}$ , $X$ is uncontrolled; 2. $Y > 0.2\text{mm}$ , not allowed;	Visual inspection, Flinka	MI
5	Pin dirty	No control	visual	MI
6	Pin scratch	Scratches and whitening are found by visual inspection, and need to be rechecked with a microscope. The broken lead is not allowed, and the overlap is not allowed Note: CT pad area and pin non-bonding area are not controlled	visual	MI
7	Screen warpage	The product is placed horizontally on the front and back, and the lifting height at one end (plug gauge) $\leq 0.3\text{mm}$	Visual inspection, plug gauge	MI
8	Color difference/stain (no convex touch)	No control	visual	MI
9	Screen body is dirty	1. The front can be wiped and the dirt can be wiped, and the polarizer of the dirt cover cannot be wiped; 2. The back is not controlled;	visual	MI
10	point defect	1. $D \leq 0.1\text{ mm}$ , $DS > 5\text{mm}$ , ignored; 2. $0.1\text{ mm} < D \leq 0.15\text{mm} \cdot N \leq 1$ ; 3. $D > 0.15\text{mm}$ , not allowed; Note: does not ship with PF film, and point/line type only controls the front	Visual inspection, Flinka	MI
11	Linear defect/foreign matter linear/non-inductive scratch	1. $W \leq 0.03\text{mm}$ , omitted; 2. $0.03 < W \leq 0.05\text{mm} \cdot L < 3.0\text{mm} \cdot N \leq 2$ ; 3. $0.05 < W \leq 0.07\text{mm} \cdot 1.0\text{mm} < L \leq 3.0\text{mm} \cdot N \leq 1$ ; 4. $W > 0.07\text{mm}$ or $L > 3\text{mm}$ , not allowed; Note: No PF film or glass is shipped, and the point/line type only controls the front	Visual inspection, Flinka	MI
12	Mixture	not allow	visual	-
13	other	The internal and external packaging shall be clean, tidy, intact and undamaged; The internal and external packaging marks are clear and accurate; The following defects are not allowed: moldy, damp, wet and damaged.	visual	-
14	Boundary dimension NG	It is not allowed to exceed the dimensional tolerance required by the specifications and drawings	Calipers, measuring instruments	-

## 8.5 Inspection picture library

Serial number	picture	Picture name	Mainly judged as defective	remarks
1		W_GRAD(64) 64 grayscale	Point/line type, foreign matter point/line, mura type	/
2		W_GRAD(128) 128 grayscale	Point/line type, foreign matter point/line, mura type	/
3		WHITE white	Point/line type, foreign matter point/line, mura type	/
4		Black black	Bright spot, bright line, dark mura	/
5		RED red	Point type, line type, foreign matter point/line	/
6		GREEN green	Point type, line type, foreign matter point/line	/
7		BLUE blue	Point type, line type, foreign matter point/line	/

## 9 Reliability Specification

Item	Condition	Cycle Time	Quantity	Remark
Constant Temp. and Constant Humidity Operation Test	+40 ± 3°C, 90 ± 3%RH	96hrs	--	
High Temp. Operation Test	+70 ± 3°C	96hrs	--	*1
Low Temp. Operation Test	-20 ± 3°C	96hrs	--	
Thermal Shock Test	-20 ± 3°C (30min) +70 ± 3°C (30min)	10cycles	--	
ESD Test(end product)	150pF, 330Ω, ±2KV, Contact 150pF, 330Ω, ±6KV, Air	10times	--	*2, *3
Vibration Test (for packaging)	Frequency: 10Hz to 55Hz to 10Hz, Swing: 1.5mm, time : X, Y, Z each 2H.	6hrs	One inner carton	*4

Note 1. For humidity test, DI water should be used.

Inspection Standard: Inspect after 1-2hrs storage at room temperature, the sample shall be free from the following defects:

- Air bubble in the LCD
- Seal Leakage
- Non-display
- Missing Segment
- Glass Crack
- IDD is greater than twice initial value.
- Others as per QA Inspection Criteria

Note 2. No defect is allowed after testing

The End Product ESD value is only indicative and depends on customer ESD protection design for the whole system.

Note 3. ESD should be applied to LCD glass panel, not other areas (such as on IC and so on)

IDD should be within twice initial value.

In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.

Note 4. Only upon request.

## 10 Precautions and Warranty

### 10.1 Safety

10.1.1 The liquid crystal in the LCD is poisonous. Do not put it in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and water.

10.1.2 Since the liquid crystal cells are made of glass, do not apply strong impact on them. Handle with care.

### 10.2 Handling

10.2.1 Reverse and use within ratings in order to keep performance and prevent damage.

10.2.2 Do not wipe the polarizer with dry cloth, as it might cause scratch. If the surface of the LCD needs to be cleaned, wipe it swiftly with cotton or other soft cloth soaked with petroleum IPA, do not use other chemicals.

### 10.3 Operation

10.3.1 Do not drive LCD with DC voltage

10.3.2 Response time will increase below lower temperature

10.3.3 Display may change color with different temperature

10.3.4 Mechanical disturbance during operation, such as pressing on the display area, may cause the segments to appear “fractured”.

### 10.4 Static Electricity

10.4.1 CMOS LSIs are equipped in this unit, so care must be taken to avoid the electro-static charge, by ground human body, etc.

10.4.2 The normal static prevention measures should be observed for work clothes and benches.

10.4.3 The module should be kept into anti-static bags or other containers resistant to static for storage.

### 10.5 Limited Warranty

10.5.1 Unless otherwise agreed between RRJ-DISPLAY and customer, RRJ-DISPLAY will replace or repair any of its LCD and LCM which RRJ-DISPLAY found to be defective electrically and visually when inspected in accordance with RRJ-DISPLAY Quality Standards, for a period of one year from date of shipment.

10.5.2 The warranty liability of RRJ-DISPLAY is limited to repair and/or replacement. RRJ-DISPLAY will not be responsible for any consequential loss.

10.5.3 If possible, we suggest you use up all modules in six months. If the module storage time over twelve months, we suggest that recheck it before the module be used.

## 11 Packaging

TBD

## 12 Prior Consult Matter

1. For IEXCELLENCE standard products, we keep the right to change material, process for improving the product property without prior notice to our customer.
2. For OEM products, if any changes are needed which may affect the product property, we will consult with our customer in advance.
3. If you have special requirement about reliability condition, please let us know before you start the test on our samples.