Tailorpixels

A Professional Manufacturer of Display

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Product Specification

Model: TOQ801XHT-02C

8.01"AMOLED Display Module(2480×1860）

This module uses RoHS material

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Record of Revision

Version	Revise Date	Page	Content
V1.0	2025/01/03		
V2.0			
V3.0			
V4.0			

Contents

1 General Description

1.1 Features

1.1.1 8.01" Flexible AMOLED Panel

1.1.2 Supported 4: 3 FHD+ (2480×1860 pixels) Resolution

1.1.3 Green Design

1.1.4 Driving Frequency: support 60Hz ;

1.2 Specifications Summary

No.	Item	Unit	Specification	Note
1	Screen size	inch	8.01	
2	Resolution	dot	2480×1860 (SPR)	
3	Display mode	--	AMOLED	
4	Aspect Ratio	--	4 : 3	
5	Active area	mm	162.688*122.016	
6	Outline Dimension	mm	165.688* 137.916	MOD W/O CG
7	Driver IC	--	RM69380	
8	Touch IC	--	FT3881	
9	IC Location	--	Driver IC : COP Touch IC : FPC	
10	Touch Sensor	--	DOT	
11	Interface	--	Drive : MIPI Touch : IIC	

2 Electrical Specifications

2.1 Main FPC Pin Assignment—AMOLED Panel Input / Output Signal Interface

Connector Type: BM035-I40-C08

Pin No.	Symbol	I/O	Description	Notes
1	ELVSS	P	AMOLED Negative Power Supply	
2	TP_SDA	I	Touch IIC Interface, Data Pin	
3	ELVSS	P	AMOLED Negative Power Supply	
4	TP_INT	I/O	TP Interrupt	
5	MTP_PWR	P	left open or connected to DVSS in normal condition	
6	TP_SCL	I/O	Touch IIC Interface, Clock Pin	
7	ELVDD	P	Not connected.	
8	TP_VDD	P	Power Supply Input for TP Analog Circuit	
9	ELVDD	P	AMOLED Positive Power Supply	
10	TP_IOVCC	P	Power Supply Input for TP Digital Circuit	
11	AVDD	P	Power Supply Input for Analog Circuit	
12	TP_RST	I	Touch Reset Pin	
13	VDDI	P	Power Supply Input for Digital Circuit	
14	GND	P	Ground	
15	VCI	P	Power Supply Input for Analog Circuit	
16	D2P	I	DSI-D2 Positive Differential Data Signals of MIPI	
17	NC	-	- Not Connected	
18	D2N	I	DSI-D2 Negative Differential Data Signals of MIPI	
19	AVDD_EN	O	AVDD_EN Signal for PMIC	
20	D1P	I	DSI-D1 Pegative Differential Data Signals of MIPI	
21	SWIRE	O	Swire Signal for PMIC	
22	D1N	I	DSI-D1 Negative Differential Data Signals of MIPI	
23	TE	I	DIC TE Signal	
24	GND	P	Ground	
25	RST	I	RESET FOR DIC	
26	CLKP	I	DSI-CLK Positive Differential Data Signals of MIPI	
27	NC	-	- Not Connected	
28	CLKN	I	DSI-CLK Negative Differential Data Signals of MIPI	
29	GND	P	Ground	
30	GND	P	Ground	
31	NC	-	- Not Connected	
32	D0P	I	DSI-D0 Positive Differential Data Signals of MIPI	
33	NC	-	- Not Connected	

Pin No.	Symbol	I/O	Description	Notes
34	DoN	I	DSI-Do Negative Differential Data Signals of MIPI	
35	NC	-	- Not Connected	
36	D3P	I	DSI-D3 Positive Differential Data Signals of MIPI	
37	NC	-	- Not Connected	
38	D3N	I	DSI-D3 Negative Differential Data Signals of MIPI	
39	NC	-	- Not Connected	
40	GND	P	Ground	
41	GND	P	Ground	
42	GND	P	Ground	
43	GND	P	Ground	
44	GND	P	Ground	
45	GND	P	Ground	
46	GND	P	Ground	

Note : I (Input); O (Output); P (Power); I/O (Input /Output);

2.2 Absolute Maximum Ratings

2.2.1 Module Panel Absolute Maximum Ratings

Item	Symbol	Value		Unit	Remark
		Min.	Max.		
Digital Power Supply	VDDIO	-0.3	3.6	V	Note1
Analog Power Supply	VCI	-0.3	5.5	V	
Power Supply For Analog Circuit.	AVDD	-0.3	9.0	V	
Digital Power Supply	DVDD	--	--	V	
ELVDD Power Supply	ELVDD	-0.3	6	V	Note2
ELVSS Power Supply	ELVSS	-9.5	-0.3	V	
Operating Temperature(Ambient)	Top	-	-	℃	Refer to RA test result
Storage Temperature(Ambient)	Tstg	-	-	℃	
Humidity	Hstg	-	-	%RH	

Note1: If the module exceeds the absolute maximum ratings, it may be damaged permanently.

Note2: PMIC (SGM3836A/NT50379WHB) Supply;

3 Electrical Characteristics

3.1 Display DC Characteristics &Current Consumption

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
ELVDD	ELVDD	-	4.55	4.6	4.65	V	Controlled By DDIC VINA=VINP=2.9V to 4.8V;
ELVSS	ELVSS	-	-3.27 -4.04	Normal : -3.3 HBM : -4	-3.33 -3.96	V	
AVDD	AVDD	-	7.52	7.6	7.68	V	
VCI	VCI	-	2.65	3.0	4.8	V	-
DVDD	DVDD	-	--	--	--	V	
VDDIO	VDDIO	-	1.65	1.8	1.95	V	-
Current Consumption	AVDD	Frame f=60Hz Normal/430nits White pattern	34.69	38.08	40.92	mA	Note1
	VCI		10.31	10.58	10.92	mA	
	VDDIO		114.6	117.97	121.86	mA	
	ELVDD		423.25	451.78	451.78	mA	
	ELVSS		-423.01	423.01	451.46	mA	
	AVDD	Frame f=60Hz HBM/600nits White pattern	34.74	37.48	40.65	mA	
	VCI		10.23	10.52	10.93	mA	
	VDDIO		115.03	118.73	122.68	mA	
	ELVDD		597.62	619.09	635.23	mA	
	ELVSS		597.41	618.89	635.15	mA	

Note1: Average of 30pcs Module Panel

3.2 Touch DC Characteristics &Current Consumption

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
AVDD	TP_VDD	-	2.7	3.3	3.3	V	
VDDIO	TP_VDDIO	-	1.65	1.8	1.95	V	
Power Consumption	Active With one finger	-	72	77.3	78.9	mW	Note1
	Active With one finger	-	81.5	81.7	81.9	mW	
	Idle Mode	-	5.7	9.9	12.3	mW	
	Sleep Mode	-	0.4	0.4	0.4	mW	
	Gesture Mode	-	5.0	7.2	8.4	mW	

Note1: Average of 30pcs Module Panel.

3.3 SPI Interface Characteristic

3.3.1 Data to Clock Timing Definitions

Table 2-2 I²C Timing Parameters

Symbol	Parameter	Min	Max	Unit
fSCL	SCL frequency		400	KHz
tBUF	Bus free time between a STOP and START condition	1.3		us
tHD;STA	Hold time (repeated) START condition After this period, the first clock pulse is generated	0.6		us
tSU;DAT	Data set-up time	100		ns
tSU;STA	Set-up time for a repeated START condition	0.6		us
tSU;STO	Set-up Time for STOP condition	0.6		us

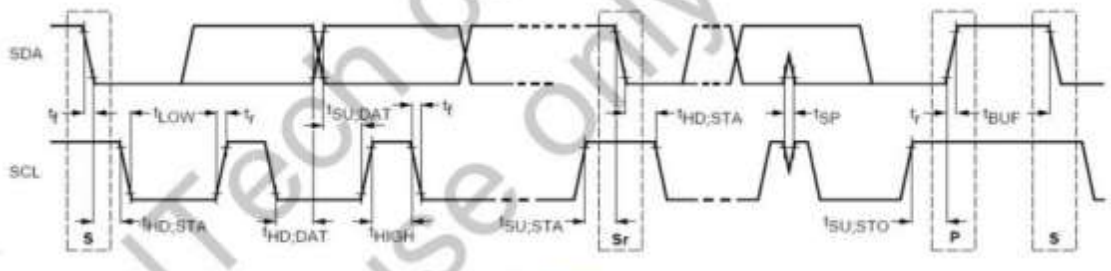


Figure 2-8 AC definition timing of the I2C interface

3.4 MIPI Interface Characteristic

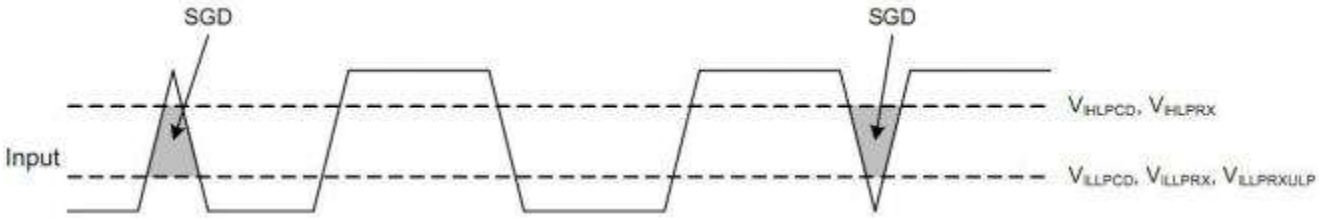
3.4.1 DC Characteristics for D-PHY LP Mode

Parameter	Symbol	Conditions	Specification			Unit
			Min.	Typ.	Max.	
Logic high level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic low level input voltage	V_{ILLPCD}	LP-CD	0	-	200	mV
Logic high level input voltage	V_{IHLPRX}	LP-RX (CLK, Do, D1)	880	-	1350	mV
Logic low level input voltage	V_{ILLPRX}	LP-RX (CLK, Do, D1)	0	-	550	mV
Logic low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0	-	300	mV
Logic high level input voltage	V_{OHLPTX}	LP-TX (Do)	1.1	-	1.3	V
Logic low level input voltage	V_{OLLPTX}	LP-TX (Do)	-50	-	50	mV
Logic high level input current	I_{IH}	LP-CD, LP-RX	-	-	10	μA
Logic low level input current	I_{IL}	LP-CD, LP-RX	-10	-	-	μA
Input pulse rejection	SGD	DSI2-CLK+/-, DSI2-Dn+/-	-	-	300	Vps

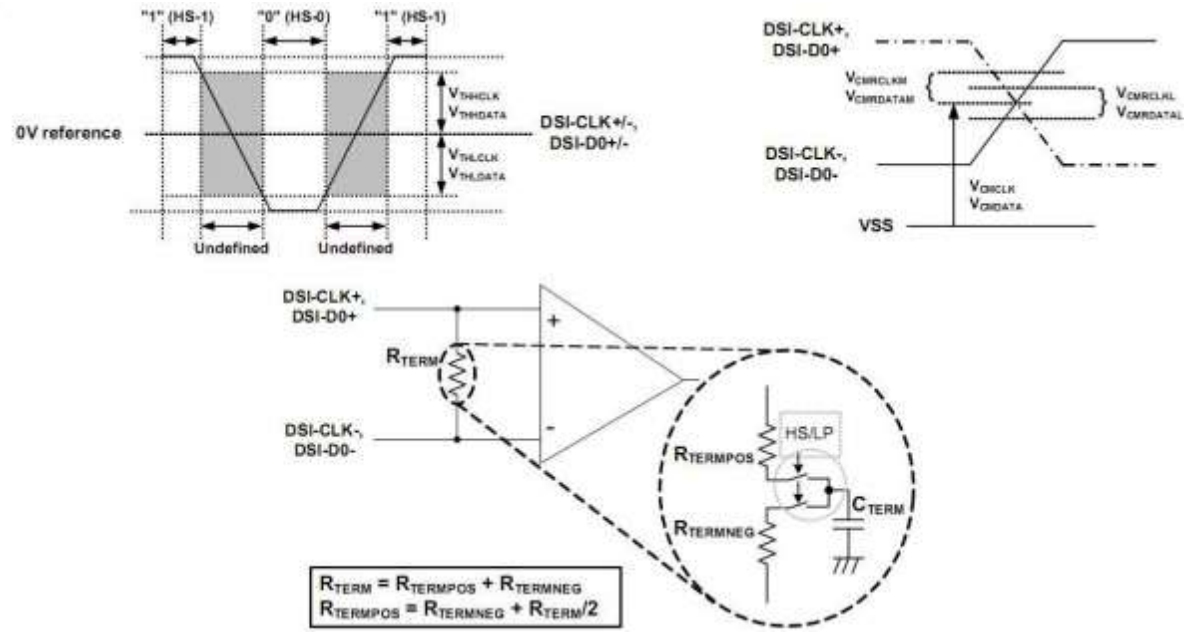
Note 1) VDDI=1.65~1. 95V, DVSS=AVSS=VSSR=VSSB=VSSAM=0V, Ta=- 30 to 70 ºC (to +85 ºC no damage).

Note 2) DSI2 high speed is off.

Note 3) Peak interference amplitude max. 200mV and interference frequency min. 450MHz.



3.4.2 DC Characteristics for D-PHY HS Mode



Parameter	Symbol		Specification			Unit
			Min.	Typ.	Max.	
Input Voltage Common Mode Range	V_{CMCLK} V_{CMDATA}	DSI2-CLK+/- - - (Note2, 3)	70	-	330	mV
Input Voltage Common Mode Variation (≤ 450MHz)	$V_{CMRCLKL}$ $V_{CMRDATAL}$	DSI2- -, DSI2- - (Note4)	-50	-	50	mV
Input Voltage Common Mode Variation (≥ 450MHz)	$V_{CMRCLKM}$ $V_{CMRDATAM}$	DSI2 - -, DSI2-Dn+/-	-	-	100	mV
Low-level Differential Input Voltage Threshold	V V	-CLK+/-, DSI2-Dn+/-	-70	-	-	mV
High-level Differential Input Voltage Threshold	V_{THHCLK} $V_{THHDATA}$	DSI2-CLK+/-, DSI2-Dn+/-	-	-	70	mV
Single-ended Input Low Voltage	V_{ILHS}	DSI2-CLK+/-, DSI2-Dn+/-	-40		-	mV
Single-ended Input High Voltage	V_{IHHS}	DSI2-CLK+/-, DSI2-Dn+/-	-	-	460	mV
Differential Input Termination Resistor	R_{TERM}	DSI2-CLK+/-, DSI2-Dn+/-	80	100	125	Ω
Single- for Termination Enable	$V_{TERM-EN}$	DSI2-CLK+/-, DSI2-Dn+/-	-	-	450	mV
Termination Capacitor	C_{TERM}	DSI2-CLK+/-, DSI2-Dn+/-	-	-	14	pF

Note 1) VDDI=1.65~1. 95V, DVSS=AVSS=VSSR=VSSB=VSSAM=0V, Ta=- 30 to 70 ºC (to +85 ºC no damage).

Note 2) Includes 50mV (- 50mV to 50mV) ground difference.

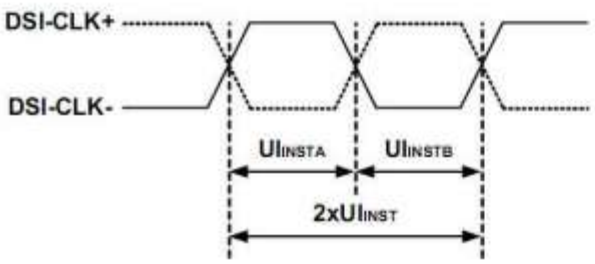
Note 3) Without VCMRCLKM / VCMRDATAM .

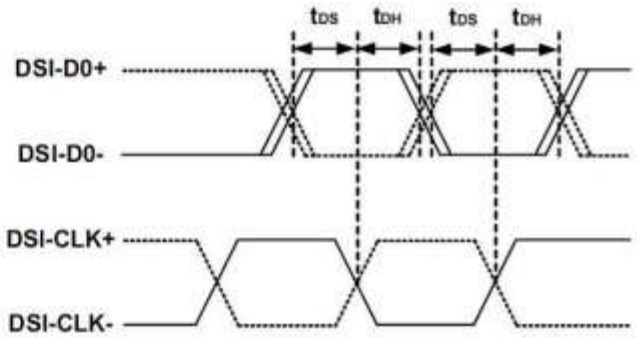
Note 4) Without 50mV (- 50mV to 50mV) ground difference.

Note 5) Dn=D0, D1, D2 and D3.

3.4.3 MIPI DSI2 Timing Characteristics

3.4.3.1 D-PHY High Speed Mode





Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
DSI2-CLK+/-	$2xUI_{INST}$	Double UI Instantaneous	1.67	-	4	ns	4 Lane (Note 2)
DSI2-CLK+/-	UI_{INSTA} UI_{INSTB}	UI Instantaneous Halfs ($UI = UI_{INSTA} = UI_{INSTB}$)	0.83	-	2	ns	4 Lane (Note 2)
DSI2-Dn+/-	tDS	Data to Clock Setup Time	0.15xUI	-	-	ps	Note 1, 3
			0.2xUI		-		Note 1, 4
DSI2-Dn+/-	tDH	Data to Clock Hold Time	0.15xUI	-	-	ps	Note 1, 3
			0.2xUI		-		Note 1, 4
DSI2-CLK+/- DSI2-Dn+/-	tDRTCLK	Differential Rise Time for Clock	-	-	0.3xUI	ps	Note 1, 5
			-	-	0.35xUI		Note 1, 6
			100	-	-		Note 1, 7

Note 1) Dn = D0, D1, D2 and D3.

Note 2) Maximum total bit rate is TBD Gbps for 24-bit data format which support to 1440RGBx3360 resolution.

Note 3) Total setup and hole window for receiver of 0. 3 UIINST when D-PHY is supporting maximum data rate = 1Gbps.*

Note 4) Total setup and hole window for receiver of 0.4 UIINST when D-PHY is supporting maximum data rate > 1Gbps.*

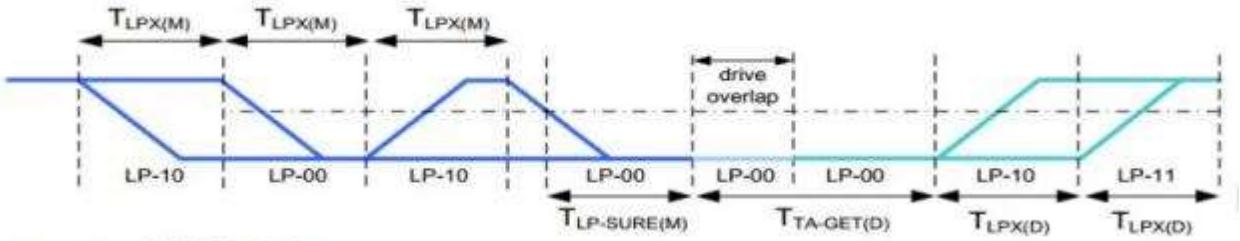
Note 5) Applicable when operating at HS bit rates ≤ 1 Gb ps (UI ≥ 1 ns).

Note 6) Applicable when operating at HS bit rates > 1 Gbps (UI < 1 ns).

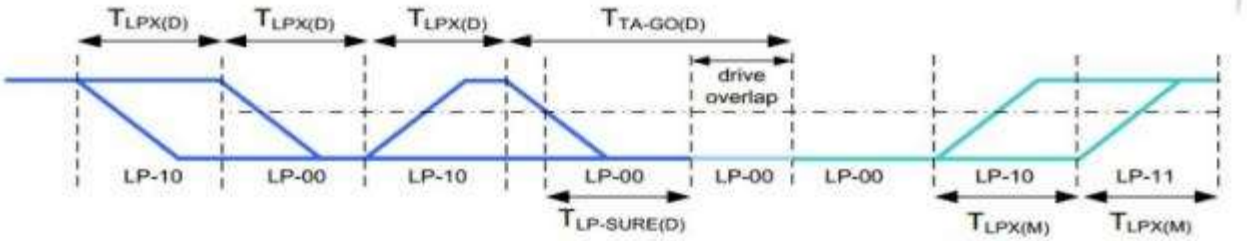
Note 7) Applicable for all HS b it rates. However, to avoid excessive radiation, b it rates ≤ 1 Gb ps (UI ≥ 1 ns), should not use values below 150 ps.

3.4.3.2 D-PHY Low Power Mode

■ Bus Turnaround Procedure (From MPU to display module)



Bus turnaround (BAT) timing



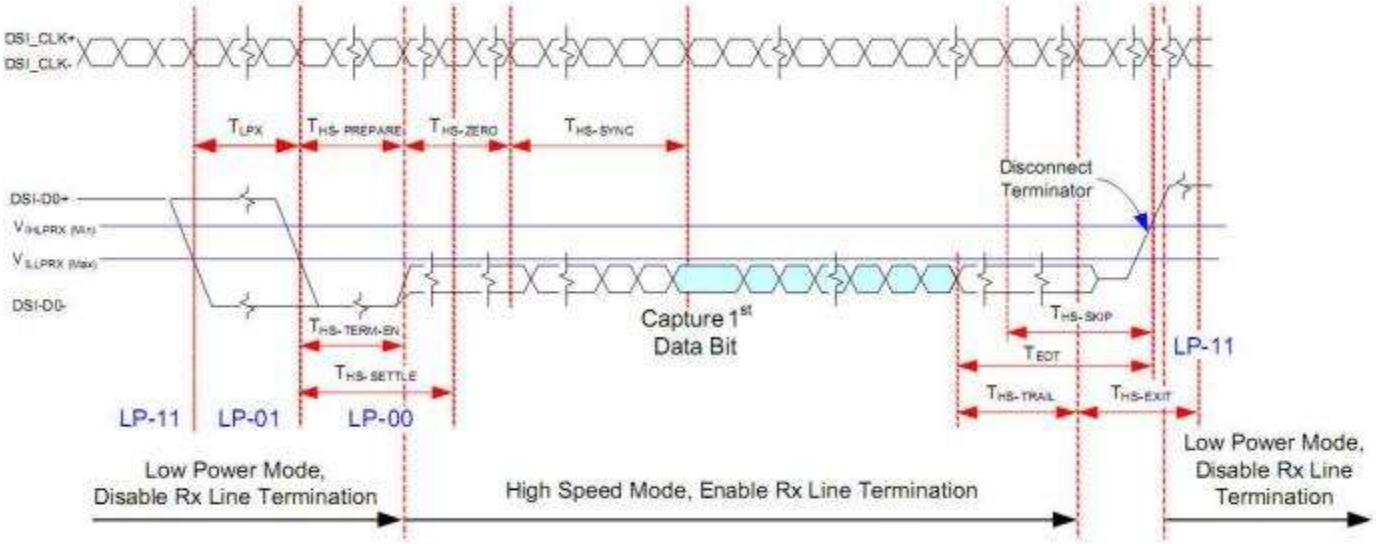
Bus turnaround (BAT) from display module to MPU timing

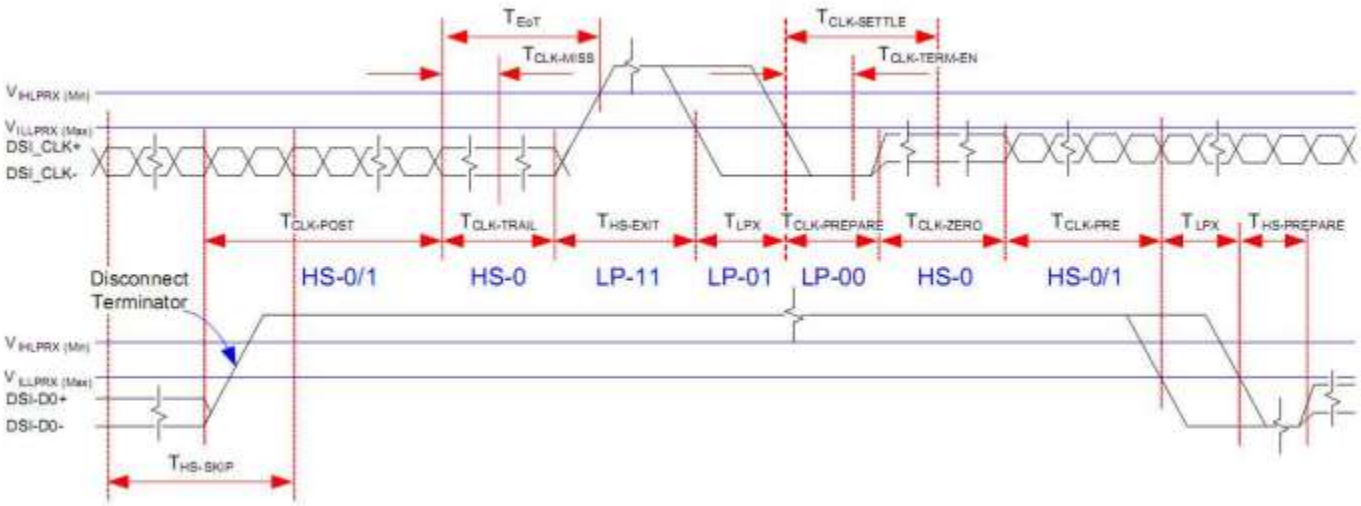
Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
DSI2-D0+/-	T_{LPXM}	Transmitted length of any Low-Power state period of MCU to display module	50	-	150	ns	1,2
DSI2-D0+/-	$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	TLPX(M)		2*TLPX(M)	ns	2
DSI2-D0+/-	T_{LPXD}	Transmitted length of any Low state period of display module to MCU	50	-	150	ns	1,2
DSI2-D0+/-	$T_{TA-SURED}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	T_{LPXD}	-	$2xT_{LPXD}$	ns	2
DSI2-D0+/-	$T_{TA-GETD}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround	-	$5xT_{LPXD}$	-	ns	2
DSI2-D0+/-	T_{TA-GOD}	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	-	$4xT_{LPXd}$	-	ns	2

Note 1) TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

Note 2) Transmitter-specific parameter.

3.4.3.3 D-PHY DSI2 Bursts





Parameter		Description	Min.	Typ.	Max.	Unit	
TCLK-POST		Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL .	60ns + 52*UI	-	-	ns	
TCLK-TRAIL		Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	-	-	ns	
THS-EXIT		Time that the transmitter drives LP-11 following a HS burst.	300	-	-	ns	
TCLK-TERM-EN		Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL, MAX .	Time for Dn to reach VTERM-EN	38	-	ns	
TCLK-PREPARE		Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	95	-	ns	
TCLK-PRE		Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	-	-	UI	
TCLK-PREPARE + TCLK-ZERO		TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	-	-	ns	
TD-TERM-EN		Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL, MAX .	Time for Dn to reach VTERM-EN	-	35 ns +4*UI		
THS-PREPARE		Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI	-	85 ns + 6*UI	ns	

THS-PREPARE + THS-ZERO		THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns + 10*UI	-	-	ns	
THS-TRAIL		Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60ns + 4*UI	-	-	ns	
t3-PREPARE		Time that the transmitter drivers the 3-wire LP-000 line state immediately before the start of the HS transmission.	38	-	95	ns	
t3-TERM-EN		Time for the slave to enable the HS line termination, starting from the time point when the A, B and C wire cross VIL_MAX.	Note 5		38	ns	
t3-SETTLE		Time interval during with the HS receiver should ignore any HS transitions on the line, starting from the beginning of t3-PREPARE.	95		-	-	
tHS-EXIT		Time that the transmitter drivers LP-111 following a HS burst.	100		-	-	
tLPRX		Transmitted length of any low-power state period	50	-	-	-	

Note 1) tLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

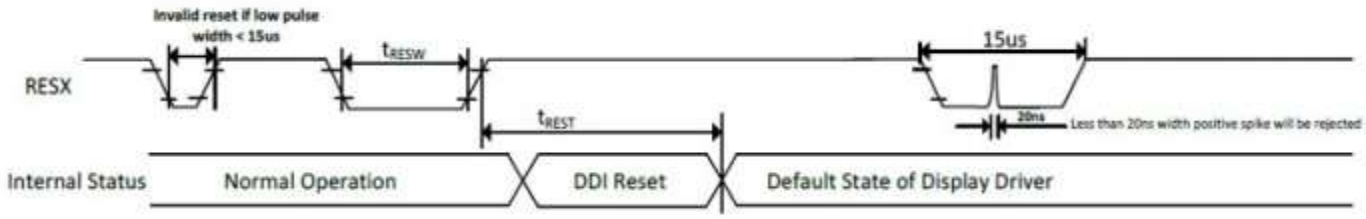
Note 2) Transmitter-specific parameter.

Note 3) Receiver-specific parameter.

Note 4) The stated values are considered informative guidelines rather than normative requirements since this parameter is untestable in typical applications.

Note 5) The receiver termination impedances shall not be enable until the single-ended voltages on all of A, B and C fall below VTERM-EN.

3.4.4 Reset Input Timing



Signal	Symbol	Parameter	Min	Typ	Max	Unit	Description
RESX	tRESW	Reset "L" pulse width	15	-	-	µs	1. Shorter than 5us, Reset rejected 2. Longer than 15us, IC reset 3. Between 5us and 15us, It depends on voltage and temperature condition.
	tREST	Reset complete time	-	-	10	ms	When reset applied during Sleep In Mode
			-	-	120	ms	When reset applied during Sleep Out Mode

Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	*Action*
Shorter than 5µs	*Reset Rejected*
Longer than 30µs	*Reset*
Between 5µs and 30µs	*Reset Start*

Note 2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In– mode) and then return to Default condition for H/W reset.

Note 3) During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

Note 4) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec

3.4.5 Touch Power On sequence

There is no restriction of power sequence. However it is recommended to turn on 1.8V earlier than 3.3V as this allows the digital core, I2C mode and firmware to be ready before AFE (charge pump and analog voltage references). But even if 1.8V and 3.3V turn on together or 3.3V turns on earlier than 1.8V, there will be no malfunction.

Fingertip touch screen controller is sharing GPI2 pin for I2C /SPI mode selection during V1V8 power On and system reset.

Name	I2C Function	SPI Function	GPI or digital input	Reset State
GPI2MODE	'1' for I2C during Reset	'0' for SPI during Reset	GPI2	MODE

The VCM1V65 pin will be 1.65V once the device is initialized and also VPUMP voltage will be 3.3V or configured output (6V).

When powering up the FTM device up or down, system design should ensure that the voltages on the signal pins in the Absolute Maximum Ratings Table are observed. Failure to follow this requirement may lead to unreliable operation of or damage to the device. Open drain signals are high impedance on power up and will transition to high once the pull up resistor voltage is present.
The GPIO and GPI pins are default input state on power up and are pulled high internally and so these do not consume any leakage current.

Double Power: VDD and VDDIO

3.5 Touch Electrical Test Item

3.5.1 Test Item

Test Item	Note
Init	TIC connection, F/W upgrade test
Pin Test	RST/INT pin connection test
Ito Test	Short test , Adjacent deviation test
Auto Tune	Capacity value calibration test
Mutual Check	Mutual capacity test, noise at power on test
Self Check	Self capacity test
Check Lockdown	Lockdown information test

3.5.2 Test Environment

1. Operator must wear the anti-ESD ring before handing.
2. The grounding condition of test fixture is well.
3. The plasma fan must be kept open during the test.
4. Do not touch the screen surface during the test, such as the fingers, the suction nozzle.

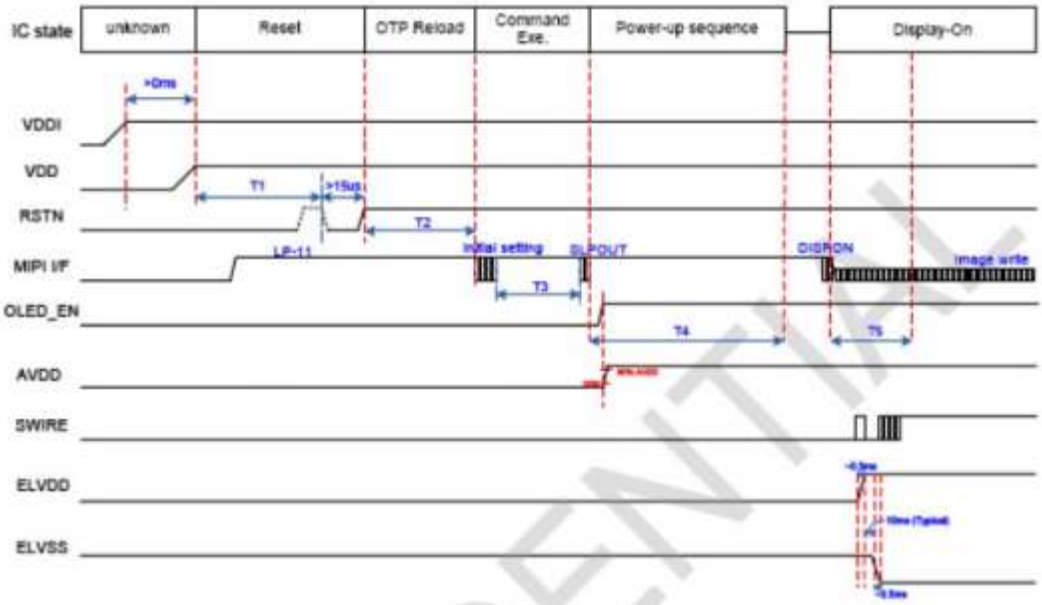
3.6 OP manual

3.6.1 Operation Sequence

3.6.1.1 Power On Sequence

提供 sequence 和上电时序图，并备注各信号间 Delay 时间要求，如下：

❖ **Power On Sequence**



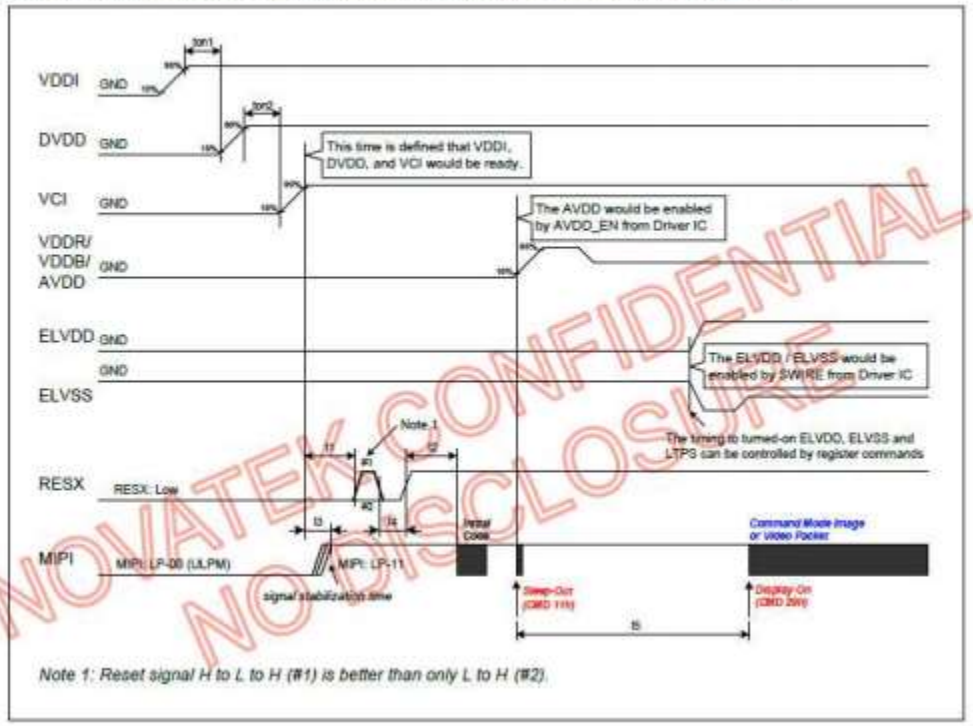
◆ **Timing Specification of Power On Sequence**

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
T1	10	-	-	ms	Effective hardware reset period
T2	10	-	-	ms	OTP reload time
T3	0	-	-	ms	Initial code input finish to SLPOUT command input
T4	-	96	-	ms	Normal power-up sequence
T5	2	-	-	VS	Display-On Blanking region

Notes: VS means the time period of a complete display frame and are approximately 16ms if internal display timing is used.

- 3 Input Power (BTM = "0") with external DVDD (EXT_DVDD_EN = "1")

VDDI=1.65~1.95V, DVDD=1.1~1.23V, VCI=2.65~4.8V, VDDR=VDDB=AVDD=6.0~8.0V

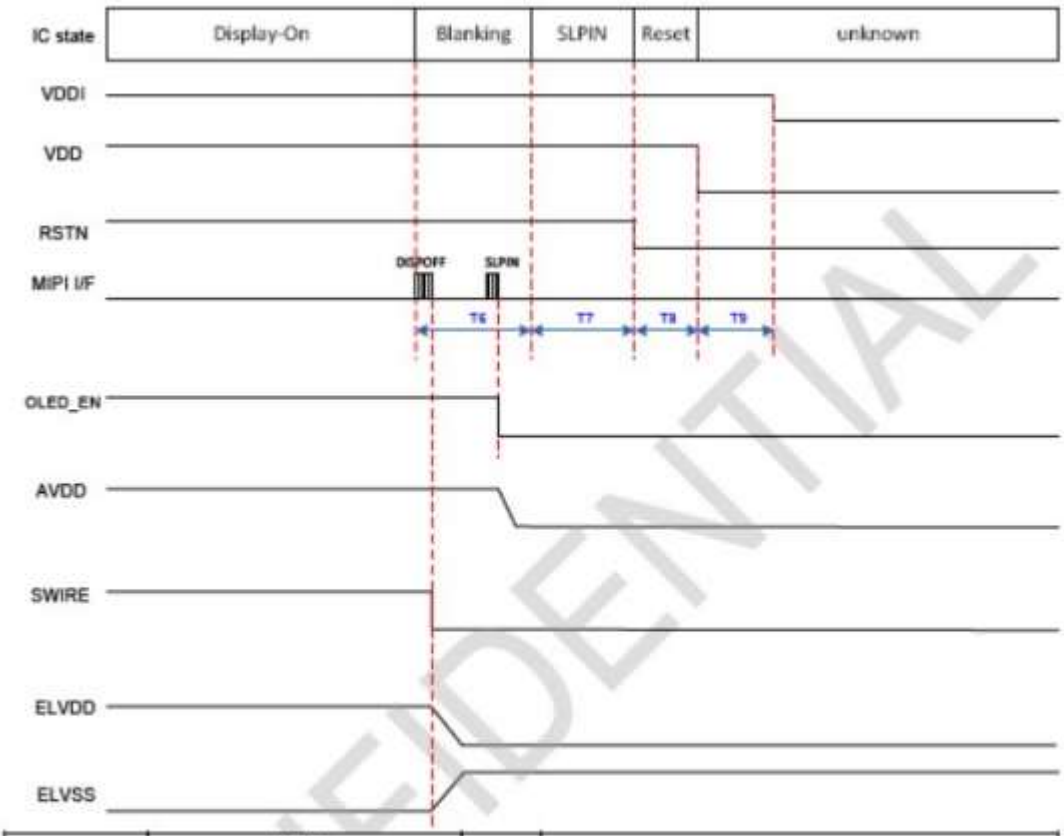


Note 1: Reset signal H to L to H (#1) is better than only L to H (#2).

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
ton1	0	-	-	ms	
ton2	-	no limit	-	ms	
t1	10	-	-	ms	
t2	10	-	-	ms	
t3	0	-	t1	ms	
t4	30	-	-	µs	
t5	120	-	-	ms	

3.6.1.2 Power off Sequence

❖ **Power Off Sequence**



Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
T6	2	-	-	VS	Display-Off blanking region
T7	1	-	-	VS	Blanking region
T8	1	-	-	ms	Effective hardware reset period
T9	2	-	-	ms	Power off period

Notes: VS means the time period of a complete display frame and are approximately 16ms if internal display timing is used.

3.6.1.3 Sleep In Sequence

Order	Sequence	Remark
1	Display On Status	
2	Display Off(28h)	
3	Wait >40ms	
4	Sleep In (10h)	
5	Sleep In Status	

3.6.1.4 Sleep Out Sequence

Order	Sequence	Remark
1	Sleep In Status	
2	Sleep Out (11h)	No.4
3	Wait>100ms	
4	Display On (29h)	
5	Display On Status	

3.6.1.5 .Deep Standby On/Off

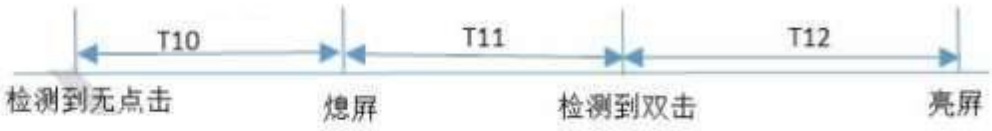
Order	Sequence	Remark
1	Display Off (28h)	No.4
2	Sleep In (10h)	No.4
3	Wait >100ms	
4	Enter Deep Standby Mode(4Fh=0x01)	
5	MIPI Drive to LP-00 or Enter ULPM	
6	In Deep Standby Mode	

3.6.1.6 双击唤醒上电时序

熄屏模式下，TIC 一直处于 Idle 或 Sleep 模式，均在上电状态，双击后，上报双击事件，由系统点亮屏幕，屏幕上电时序参考 3.1。

3.6.1.7 双击唤醒下电时序

检测到无点击，屏幕按照 3.2 power off 时序下电，TIC 将一直处于工作模式。



Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
T10	-	-	-	ms	可由整机系统设定
T11	500	-	-	ms	可由整机系统设定
T12	-	-	-	ms	可由整机系统设定

4 Optical Specification（总成测试）

Item	Symbol	Condition	Values			Unit	Notes
			Min.(≥)	Typ.	Max.(≤)		
Color shift	Δu' v'	Up/Down/Right/Left θ=30°	/	/	3.5	JNCD	Note1 Note2
		Up/Down/Right/Left θ=45°	/	/	5.5		
		Up/Down/Right/Left θ=60°	/	/	6		
Contrast ratio	CR	@0 degree	600,000 : 1	/	/	/	
Viewing angle	CR	@80 degree	1000 : 1	/	/	/	
HBM mode color chromaticity equal to normal mode	RGBWΔx	CIE1931 x	-0.005	0	0.005	/	HBM : 600nit
	RGBWΔy	CIE 1931 y	-0.005	0	0.005	/	
AOD mode color chromaticity equal to normal mode	RGBWΔx	CIE1931 x	-0.008	0	0.008	/	
	RGBWΔy	CIE 1931 y	-0.008	0	0.008	/	
'Color chromaticity (CIE1931)	Wx	CIE1931 x	0.290	0.300	0.310	/	
	Wy	CIE 1931 y	0.305	0.315	0.325		
	Rx	CIE1931 x	0.663	0.683	0.703		
	Ry	CIE 1931 y	0.297	0.317	0.337		
	Gx	CIE1931 x	0.213	0.243	0.273		
	Gy	CIE 1931 y	0.69	0.72	0.75		
	Bx	CIE1931 x	0.104	0.134	0.164		
	By	CIE 1931 y	0.026	0.056	0.065		
Color Gamut	/	DCI P3	98(>)	100	/	%	CIE1931
Luminance (complete machine)	L	/	387	430	473	nits	
HBM Luminance (complete machine)	L	/	540	600	660	nits	
AOD Luminance (complete machine)	L	/	54	60	66	nits	
Reflectivity	reflectivity	/	/	/	6	%	Re: min5.20% max5.41% ave5.28% a: min1.53 max1.87 ave1.67 b: min-2.63 max-178 ave-2.06 @DVT4
	a	L*a*b	-2.5	0	2.5	/	
	b	L*a*b	-3.0	0	3.0	/	
Response time (first frame on+off)	/	/	/	/	2	ms	
The brightness of first frame	/	/	80	/	/	%	GIR off
Color uniformity	U%	/	/	/	2	JNCD	@W255 , W128 , W64
Luminance uniformity	U%	/	80	/	/	%	

Item	Symbol	Condition	Values			Unit	Notes
			Min.(≥)	Typ.	Max.(≤)		
Crosstalk	/	IEC	/	/	2	%	
'IR-Drop	/	|(R+G+B) - W|/W	/	/	6	%	
Lifetime@T95	/	/	400	/	/	Hr	W Pattern
	Δu' v'	/	/	/	0.004	/	
Gamma	/	L5~L232	2.0	2.2	2.4	/	HBM：600nit
		L233~L240	1.9	2.2	2.5	/	
		L5~L232	2.0	2.2	2.4	/	100nit＜L255≤430nit
		L233~L240	1.9	2.2	2.5	/	
		L13~L227	2.0	2.2	2.4	/	10nit＜L255≤100nit
		L228~L235	1.9	2.2	2.5	/	
		L25~L222	2.0	2.2	2.4	/	2nit≤L255≤10nit
		L223~L230	1.9	2.2	2.5	/	
		L13~L227	2.0	2.2	2.4	/	AOD：60nit
		L228~L235	1.9	2.2	2.5	/	
Color shift of white pattern in different DBV register value	Δu' v'	Condition1	/	/	0.004	/	L255 满足左侧需求
	CCT	Condition2	/	/	400	K	
Image Sticking	/	The Time to < 1 JND(0.004)	/	20	25	s	Panel Add Cu
	/	18*6 checker pattern 10min，to G128	/	58	65	min	

Note1： Internal control, to ensure that large Angle of view to the direction of green.

Note2：视角超规部分以主观限样为准；

Test Conditions:

Condition1：max(duv of (DBV level min- max))-min (duv of(DBV level min- max))，DBV level 1=2nits；

Condition2： max(CCT of (DBV level min- max))-min(CCT of(DBV level min- max))，DBV level 1=2nits；

Condition3： The ambient temperature is 25℃,in dark room

Condition4： The test systems refer to Note 2.

Note 1 : Definition of optical measurement system.

The optical characteristics should be measured in dark room. The optical properties are measured at the center point of the OLED screen. (Gamma is measured by CA410. Reflectivity is measured by lambda 750. Lifetime is measured by lifetime equipment. Response time is measured by Eldim optiscope200. Other items are measured by CS2000A/ 1º spot diameter 7.8mm /Height: 500mm.)

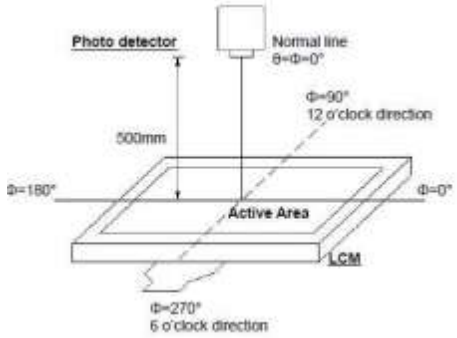
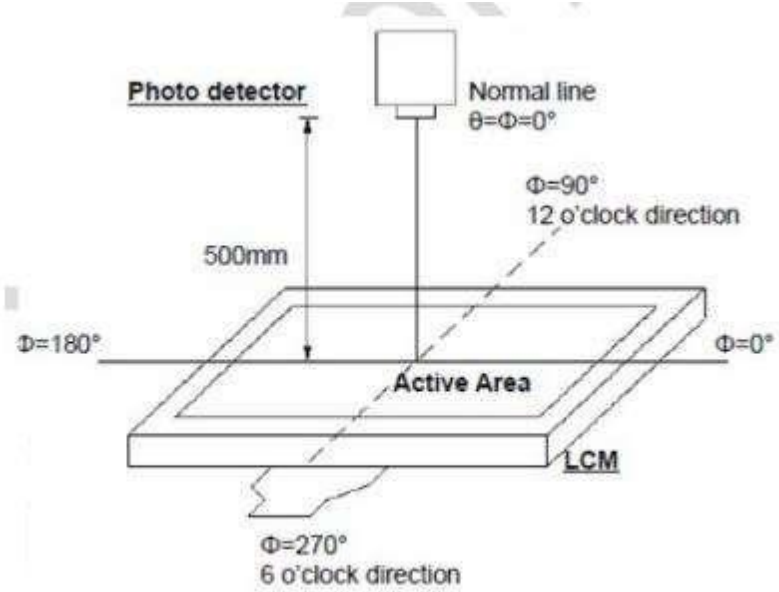


Fig 1 Definition of optical measurement system(CS2000A)

Note 2 : Definition of optical measurement system.

The optical characteristics should be measured in dark room. The optical properties are measured at the center point of the OLED screen. (Viewing angle is measured by CS2000A/Height :500mm, Response time is measured by Eldim optiscope200, other items are measured by CS2000A/ spot diameter 8mm /Height: 500mm.)



Note 3 : Definition of contrast ratio

Contrast ratio (CR) = Luminance measured when OLED on the "White" state/ Luminance measured when OLED on the "Black" state

Note 4 : Definition of color chromaticity

White/Red/Green/Blue Color coordinates measured at center point of OLED.

Note 5 : Definition of Luminance

White 255 Gray measured at center point of OLED.

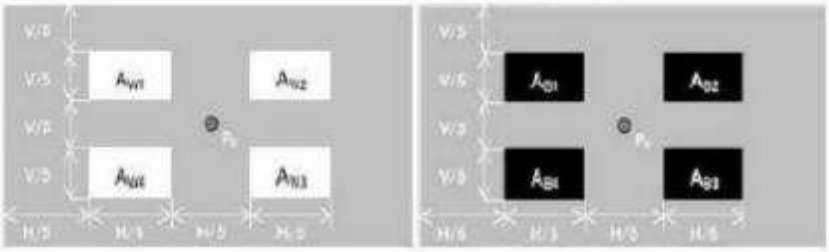
Note 6 : Definition of cross-talk

Measure luminance at the position, P o

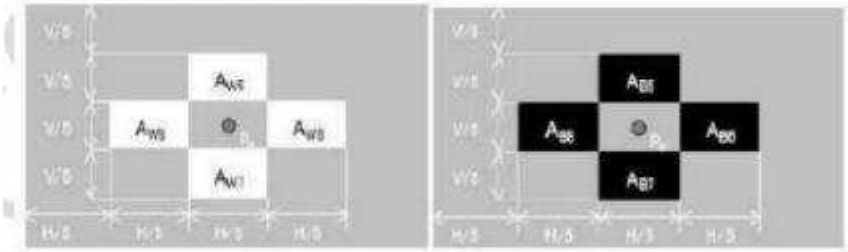
Calculate cross-talk as below equation

$$crosstalk = \frac{|L_{Wi\_ON} - L_{W\_OFF}|}{L_{W\_OFF}} \times 100\% \quad (i = 5\ to\ 8)$$

$$crosstalk = \frac{|L_{Bi\_ON} - L_{B\_OFF}|}{L_{B\_OFF}} \times 100\% \quad (i = 5\ to\ 8)$$



(a) L_{W_OFF}, L_{B_OFF} measuring pattern



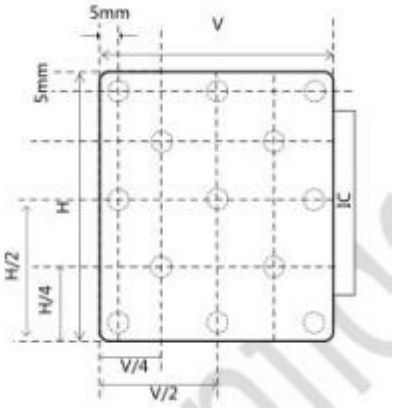
(b) L_{W_ON}, L_{B_ON} measuring pattern

Note 7 : Definition of Luminance Uniformity and color uniformity

Measure the luminance of gray level 255 &128&64 at 13 points

$$\text{Luminance Uniformity} = \frac{Lmin}{Lmax} * 100\%$$

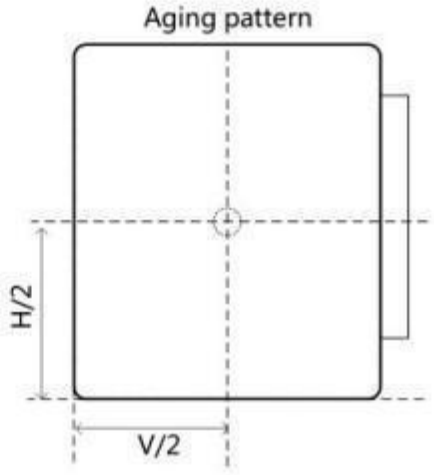
Color Uniformity=max[sqrt ((ui-uj)^2 + (vi-vj)^2)],i=1,2,3...13,j=1,2,3...13



Note 8 : Definition of Lifetime

Lifetime Measure Steps :

- Light on W Aging pattern for 0.5h befor lifetime measure
- 0h ——W Aging pattern,measure pt.① initial luminance & $\Delta u'v'$
- 0~1h ——W Aging pattern
- 1h ——W Aging pattern,measure pt ① luminance & $\Delta u'v'$
- Loop step below progress ....to 400h

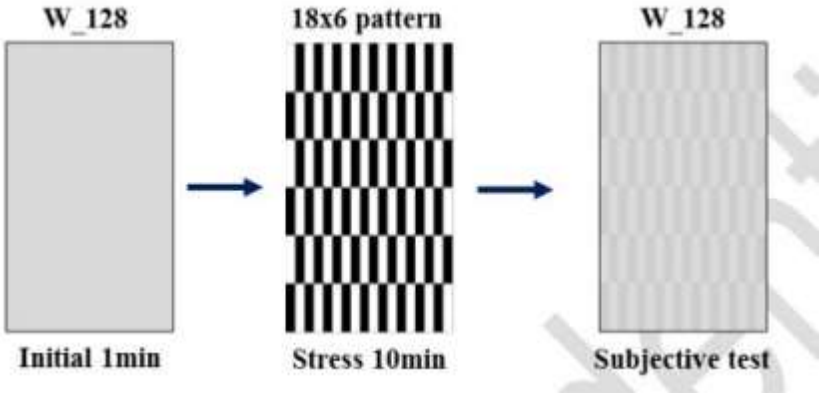


Note 9 : Definition of Image sticking

9.1 Subjective test

1. Test environment temperature is 25℃.

2. Light on W128 pattern for 1min, then change to 18*6 checker pattern for 10min, at last change to W128 pattern and record the time of duration.



9.2 Objective test

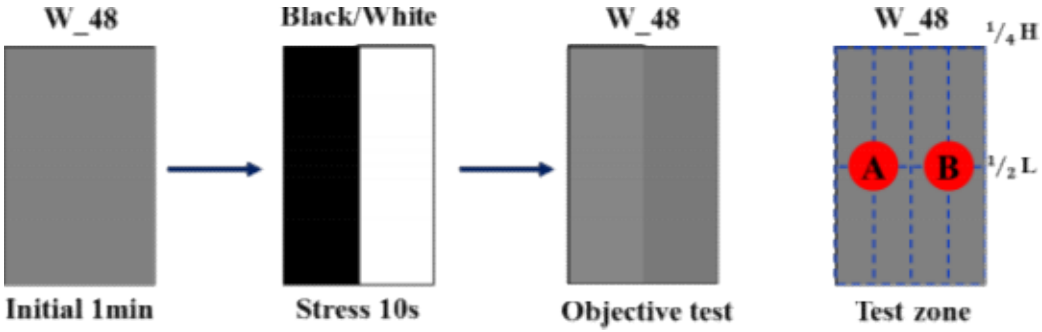


Fig 7 Definition of Objective test pattern

Step:

1. Test environment temperature is 25℃.

2. Light on 48 gray pattern for 1min, than Change to a black/white pattern for 10s, at last change the pattern back to 48 gray.

3. Using CA-P410 measures the luminance once a second of test zone in the whole process.

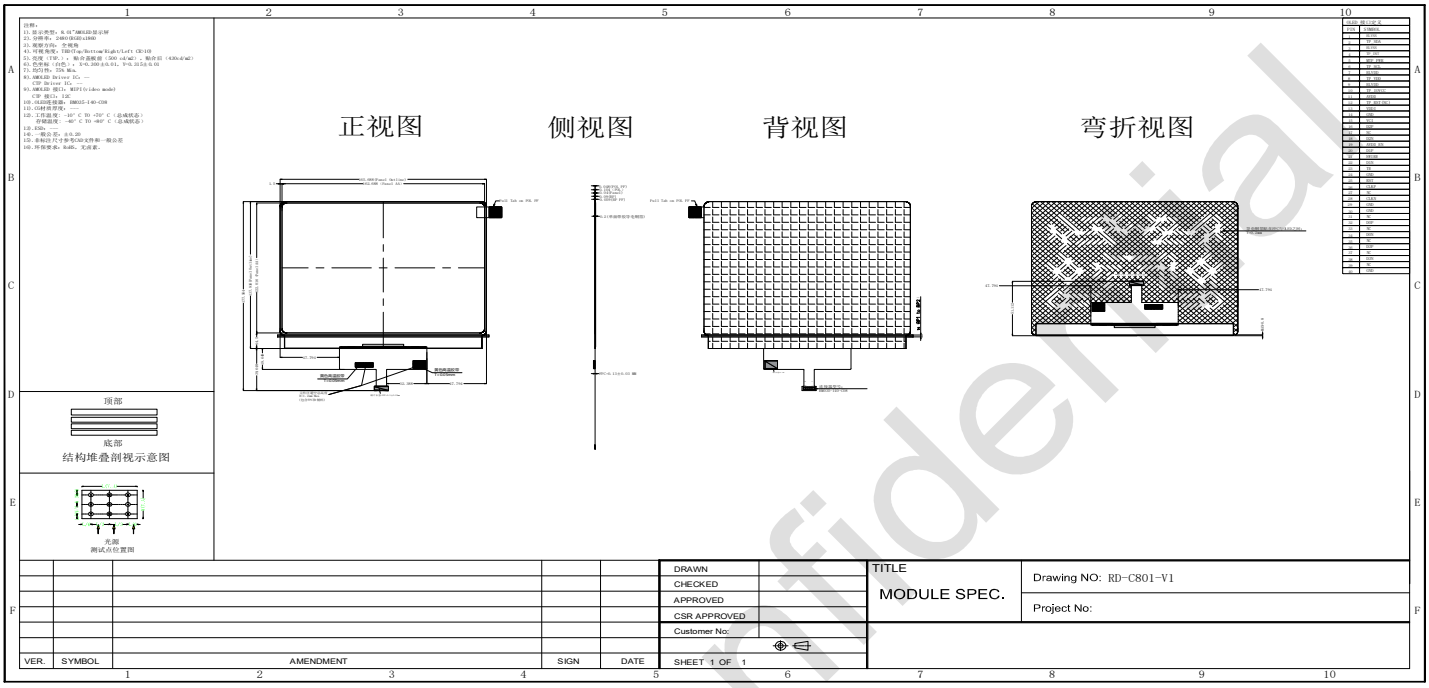
4. Calculate the Michelson contrast value X with formula below:

$$X = \left(\frac{L_{A(t)} - L_{B(t)}}{L_{A(t)} + L_{B(t)}} - \frac{L_{A(Initial\ average)} - L_{B(Initial\ average)}}{L_{A(Initial\ average)} + L_{B(Initial\ average)}}\right)/1JND$$

$$1\ JND = 0.4\%$$

5 Mechanical Characteristics

5.1 Outline Drawing



6 Package Drawing

6.1 Packing Specifications

Item	Specification	Remark
Carton(Box) Packing		
Carton(Box) Packing Size		
Carton(Box) Packing Weight		For Reference
Pallet Packing		
Pallet Packing Size		
Pallet Packing Weight		For Reference

6.2 Packing Method

TBD

6.3 quality guarantee period

Item	Spec.
quality guarantee period	Six month
Storage environment	Temperature 25 ± 5 ℃, humidity 50% ± 20%

7 RA Requirements(总成状态)

No.	Test Item	Test Condition
1	High Temperature High Humidity Operation	60℃, 90%RH ,240h
2	High Temperature Operation	70℃,240H
3	Low Temperature Operation	-10℃,240H
4	High Temperature Storage	80℃,240H
5	Low Temperature Storage	-40℃,240H
6	Thermal Shock	(-40℃/60min<->85℃/30min)，32cycles
7	ESD Test	Contact，±6KV；Air，±8KV
8	On off test	25℃±2℃，On 3s，Off 3s，1500 times
9	正面点压测试	取 9 个点以 2±0.5N 压力进行 80 万次点击，点击速率 1S/次
10	表面硬度	750g 速度 60mm/min，移动 2-3cm，划 5 条线，每划一次将铅笔芯转动 60 度
11	耐摩擦	施加 1kg 的负载，以 40cycle/min 的速度，以 40mm 的行程，压头大小:10mm*10mm，在非油墨面的表面来回磨擦 2000 个往复
12	落笔	晨光 K35 笔重 13g，点位跌落高度从 1cm 起，并以 1cm 为 step 递增，重复测试同一点位，直至 panel 出现外观及功能性不良，
13	落球	刚球重 32.65g，直径为 20mm，点位跌落高度从 1cm 起，并以 1cm 为 step 递增或递减，重复测试同一点位，直至 panel 出现外观及功能性不良，
14	Static Folded (Room temperature)	240h
15	Static Folded (60°C/90%)	60°C/90% 240h

<table>
<tr><td>16</td><td>Dynamic Folding</td><td>200K</td></tr>
<tr><td>17</td><td>Dynamic Folding (70°C)</td><td>70°C 100K</td></tr>
<tr><td>18</td><td>Dynamic Folding (-10°C)</td><td>-10°C 50K</td></tr>
<tr><td>19</td><td>Dynamic Folding (60°C/90%)</td><td>60°C/90% 100K</td></tr>
<tr><td>20</td><td>Package Test</td><td>50℃ 80%RH, Storage 2hr
Vibration Test : Frequency 5Hz , Amplitude 20mm.
Direction: X,Z; X and Z each 60min.
Package Drop Test (Direction) : 1Angle, 3Edge, 6Face;
Drop height refer to the table as below.
<table>
<tr><th>包装总重量</th><th>跌落高度 (CM)</th></tr>
<tr><td>10KG以下</td><td>80</td></tr>
<tr><td>10KG~20KG</td><td>60</td></tr>
<tr><td>20KG~30KG</td><td>50</td></tr>
<tr><td>30KG~40KG</td><td>40</td></tr>
</table>
</td></tr>
</table>

8 General Precautions

Please pay attention to the following items when you use the folding OLED Module(Panel):

8.1 Do not twist or bend the module(panel) and prevent the unsuitable external force for display during assembly.

8.2 Adopt measures for good heat radiation. Be sure to use the module(panel) with in the specified temperature.

8.3 Avoid alcohol, oil and dust mixing during assembly.

8.4 Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the module(panel).

8.5 Less EMI: it will be more safety and less noise.

8.6 Please operate module(panel) in suitable temperature. The response time & brightness will drift by different temperature.

8.7 Avoid to display the fixed pattern (exclude the white pattern) in a long period, otherwise, it will cause image sticking.

8.8 Please be sure to turn-off the power when connecting or disconnecting the circuit.

8.9 PF scratches easily, please handle it carefully.

8.10 Display surface never likes dirt or stains.

8.11 A dew drop may lead to destruction. Please wipe off any moisture before using module(panel).

8.12 Sudden temperature changes cause condensation, and it will cause polarizer damaged.

8.13 High temperature and humidity may degrade performance. Please do not expose the module(panel) to the direct sunlight and so on.

8.14 Acetic acid or chlorine compounds are not friends with AMOLED display module(panel).

8.15 Static electricity will damage the module(panel), please do not touch the module(panel) without any grounded device.

8.16 Please avoid any static electricity damage (ESD) during producing and operating.

8.17 Do not disassemble and reassemble the module(panel) by self.

8.18 Be careful do not touch the rear side directly.

8.19 No strong vibration or shock. It will cause module(panel) broken.

8.20 Store the module in a dark room where must keep at 25±10℃ and 65%RH or less.

8.21 Do not store the module in surroundings containing organic solvent or corrosive gas.

8.22 Be careful of injury from a broken display module (panel).

8.23 Please avoid the pressure adding to the surface (front or rear side) of module(panel), because it will cause abnormal display.

8.24 Do not bend the module(panel) by hand before assembly, It will cause module(panel) damage.

8.25 Do not irradiate the module(panel) directly with UV, otherwise it will cause abnormal display.

8.26 The module(panel) cannot be bent with protective film, otherwise it may cause abnormal display.

8.27 In the process of module(panel) assembly, the process protective film should be pasted, but there should be no attached bubbles, otherwise the bubbles will have the risk of imprint transfer.