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CERT. No.: 282Q19070712006



CERT. No.: 282E19070712007

Product Specification

Model: TTX134XVT-01CG

13.4" TFT Display Module(1200*1920)

This module uses RoHS material

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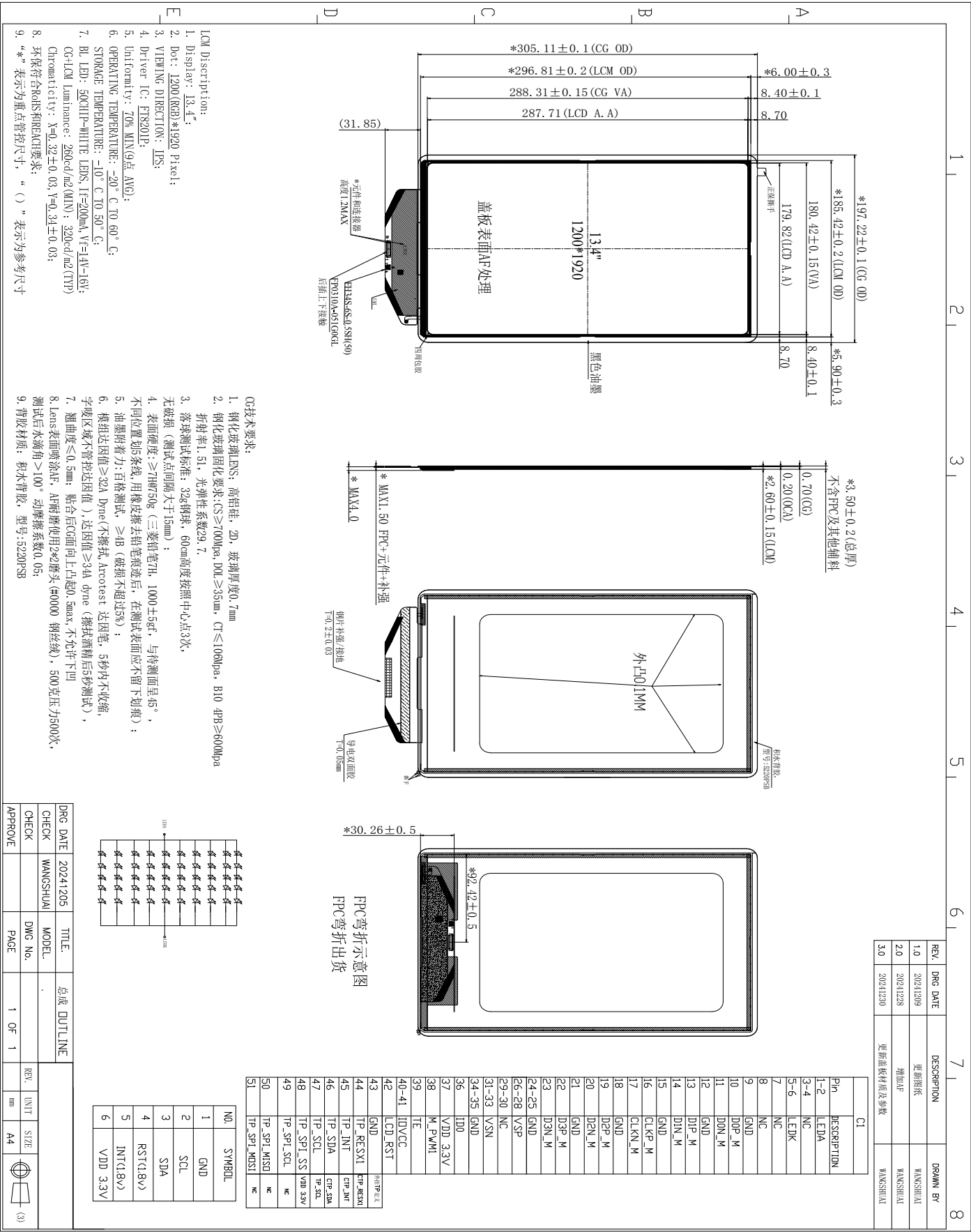
Revision History

Date	Rev.	Page	Description
2024-12-28	1.0	All	First issue

1. General Features

Item	Spec	Remark
Display Mode	Normally Black transmissive	
Gray Scale Inversion Direction	ALL o'clock	
Input Signals	MIPI + IIC	
Outside Dimensions	197.22(W)×305.11(H)×3.5(D)	mm; With CG
Active Area	179.82(W)×287.71(H)	mm
Number of Pixels	1200×RGB×1920 Pixels	
Dot Pitch	149.85(H) × 149.85(V)	um
Pixel Arrangement	RGB Vertical Stripes	
Drive IC	FT8201P	

2.Outline Dimension



3. Reliability and Inspection Standard

1	High Temperature	Storage	60℃, 96Hrs	Inspection after 2-4hours storage at room temperature,the samples should be free from defects: 1,Air bubble in the LCD. 2,Seal leak. 3,Non-display. 4,Missing segments. 5,Glass crack. 6,Current IDD is twice higher than initial value. 7,The surface shall be free from damage.
		Operation	50℃, 96Hrs	
2	Low Temperature	Storage	-20℃, 96Hrs	
		Operation	-10℃, 96Hrs	
3	High Temperature and High Humidity		40℃, 90%RH, 48Hrs	
4	Temperature Cycle(storage)		-10 ~ 50℃, 1H/cycle , Total 10 Cycles,	
REMARK: 1,The Test samples should be applied to only one test item. 2,Sample for each test item is 5pcs. 3,For Damp Proof Test, Pure water(Resistance> 10MΩ)should be used. 4,Failure Judgment Criterion: Basic Specification Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.				

4.LCM Description

4.1 Absolute Maximum Ratings

The following are maximum values which, if exceeded may cause operation or damage to the unit.

(AVDD = 4.5V ~ 6.5V, AVEE = -4.5V ~ -6.5V, VDDI = 1.65V ~ 1.95V, Ta = -30°C ~ 85°C)

Parameter	Symbol	Rating	Unit	Note
Power Supply Voltage 1	VDDI-VSS	-0.3 ~ +1.95	V	
Power Supply Voltage 2	VDD-VSS	-0.3 ~ +1.35	V	
Power Supply Voltage 3	AVDD-VSS	-0.3 ~ +6.5	V	
Power Supply Voltage 4	VSS-AVEE	-0.3 ~ +6.5	V	
Power Supply Voltage 5	VGH-VGL	-0.3 ~ +32	V	
Input Voltage	Vt	-0.3 ~ VDDI+0.3	V	

Note1. The maximum applicable voltage on any pin with respect to 0V.

Note2. Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

4.2 Electrical Specification

4.2.1 Driving TFT LCD Panel

Item		Sym.	Min	Typ.	Max	Unit	Note
I/O and Logical power		IOVCC	1.65	1.8	1.95	V	
Analog supply power		VSP	5.6	5.8	6.0	V	
		VSN	-6.0	-5.8	-5.6		
Logic Input Voltage	Low Voltage	V _{IL}	0	-	0.3IOVCC	V	
	High Voltage	V _{IH}	0.7IOVCC	-	IOVCC	V	
Logic Output Voltage	Low Voltage	V _{OL}	0	-	0.2IOVCC	V	
	High Voltage	V _{OH}	0.8IOVCC	-	IOVCC	V	

4.2.2 Driving Backlight

Item	Sym.	Min	Typ.	Max	Unit	Note
Backlight driving voltage	V _F	14	-	16	V	
Backlight driving current	I _F	-	200	-	mA	
Backlight Power Consumption	W _{BL}	-	-	-	mW	
Life Time	-	10,000	20,000	-		Note 3

Note 1: (Unless specified, the ambient temperature Ta=25℃)

Note 2: The recommended operating conditions refer to a range in which operation of this product is guaranteed. Should this range is exceeded, the operation cannot be guaranteed even if the values may be without the absolute maximum ratings.

Note 3: If LED is driven by high current, high ambient temperature & humidity condition. The life time of LED will be reduced. Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.

4.3 Optical Specifications

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 30 minutes in a dark environment at 25 °C. The values specified are at an approximate distance 500mm from the LCD surface at a viewing angle of Φ and θ equal to 0°.

Item	Sym.	Values			Unit	Note
		Min.	Typ.	Max.		
1) Contrast Ratio	C/R	1000	1500	-		FIG.1
2) Luminance Uniformity	δ WHITE	70	75	-	%	Note5
3) TCM Luminance	L	-	320	-	cd/m ²	FIG.1
4) Response time	Tr+Tf	-	-	35	ms	FIG.2
5) Viewing Angle	Θ_L	-	80	-	Degree	FIG.3
	Θ_R	-	80	-		
	Θ_U	-	80	-		
	Θ_D	-	80	-		
6) Chromaticity	Wx	Typ-0.03	0.32	Typ+0.03		FIG.1
	Wy		0.34			
	Rx		TBD			
	Ry		TBD			
	Gx		TBD			
	Gy		TBD			
	Bx		TBD			
	By		TBD			
7) NTSC	CIE1931	55	60	--	%	FIG.1

◆ Measurement System

Notes:

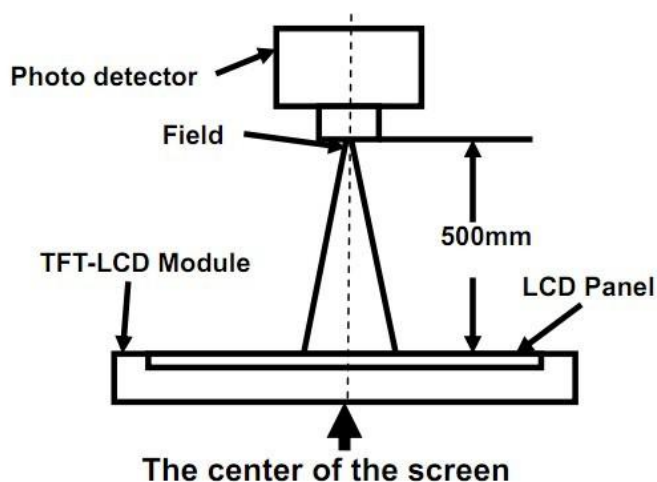
1. Contrast Ratio(CR) is defined mathematically as :

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

2. Surface luminance is the center point across the LCD surface 500mm from the surface with all pixels displaying white. For more information see FIG 1.
3. Response time is the time required for the display to transition from white to black (Rising Time, Tr) and from black to white (Falling Time, Tf). For additional information see FIG 2.
4. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG 3.
5. The uniformity in surface luminance (δ WHITE) is determined by measuring luminance at each test position 1 through 9, and then dividing the maximum luminance of 9 points luminance by minimum luminance of 9 points luminance.

$$\delta \text{ WHITE} = \frac{\text{Minimum Surface Luminance with all white pixels}}{\text{Maximum Surface Luminance with all white pixels}}$$

FIG. 1 Optical Characteristic Measurement Equipment and Method



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

FIG. 2 The definition of Response Time

The response time is defined as the following figure and shall be measured by switching the input signal for “black” and “white”.

Response Time = Rising Time(T_r) + Falling Time(T_f)

- Rising Time(T_r) : Full White 90% → Full White 10% Transmittance.
- Falling Time(T_f) : Full White 10% → Full White 90% Transmittance.

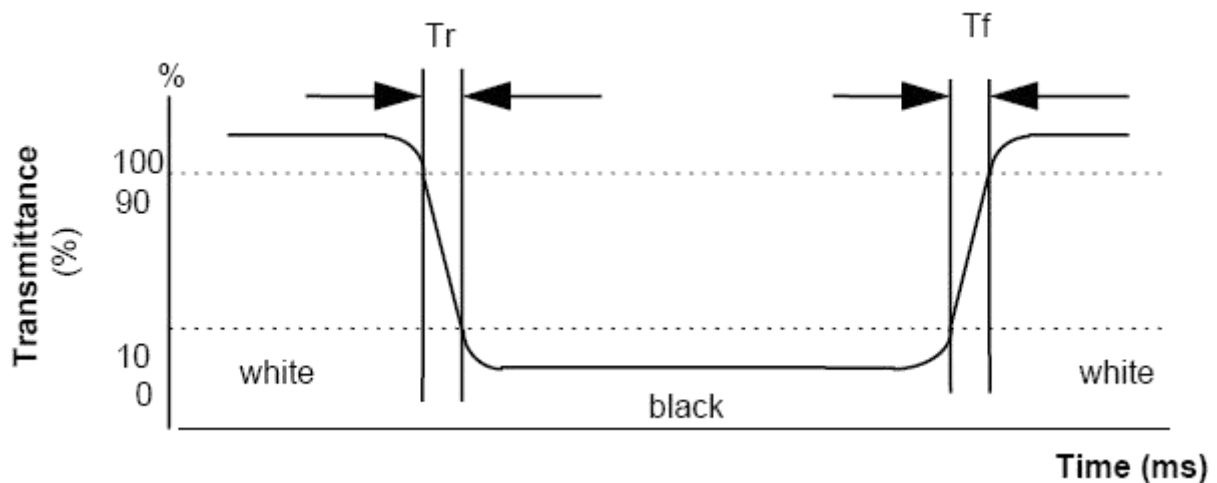
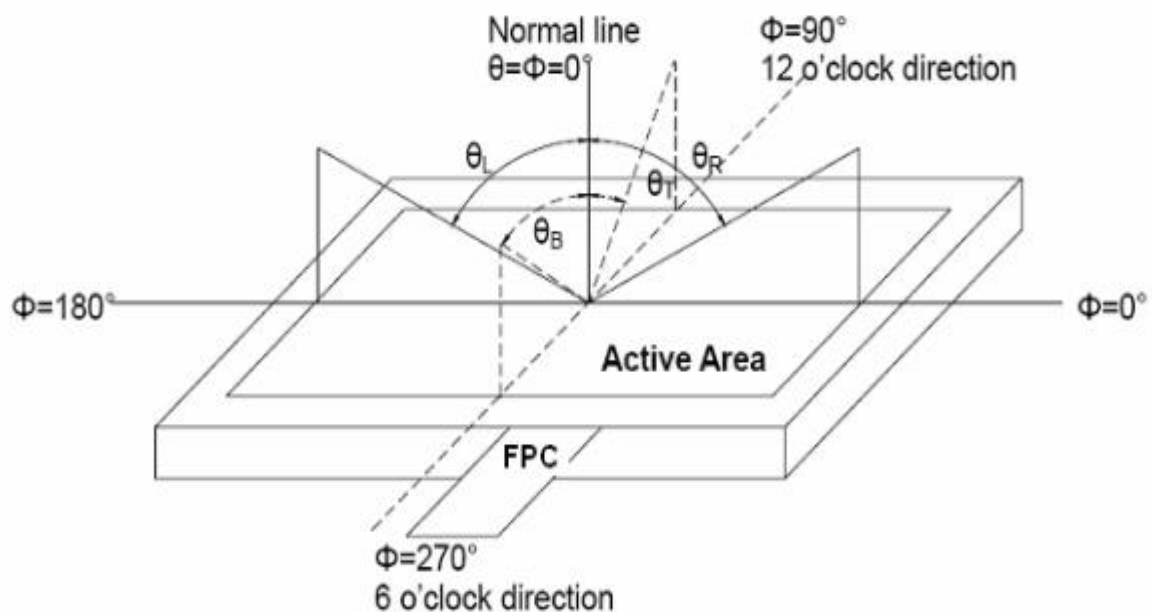
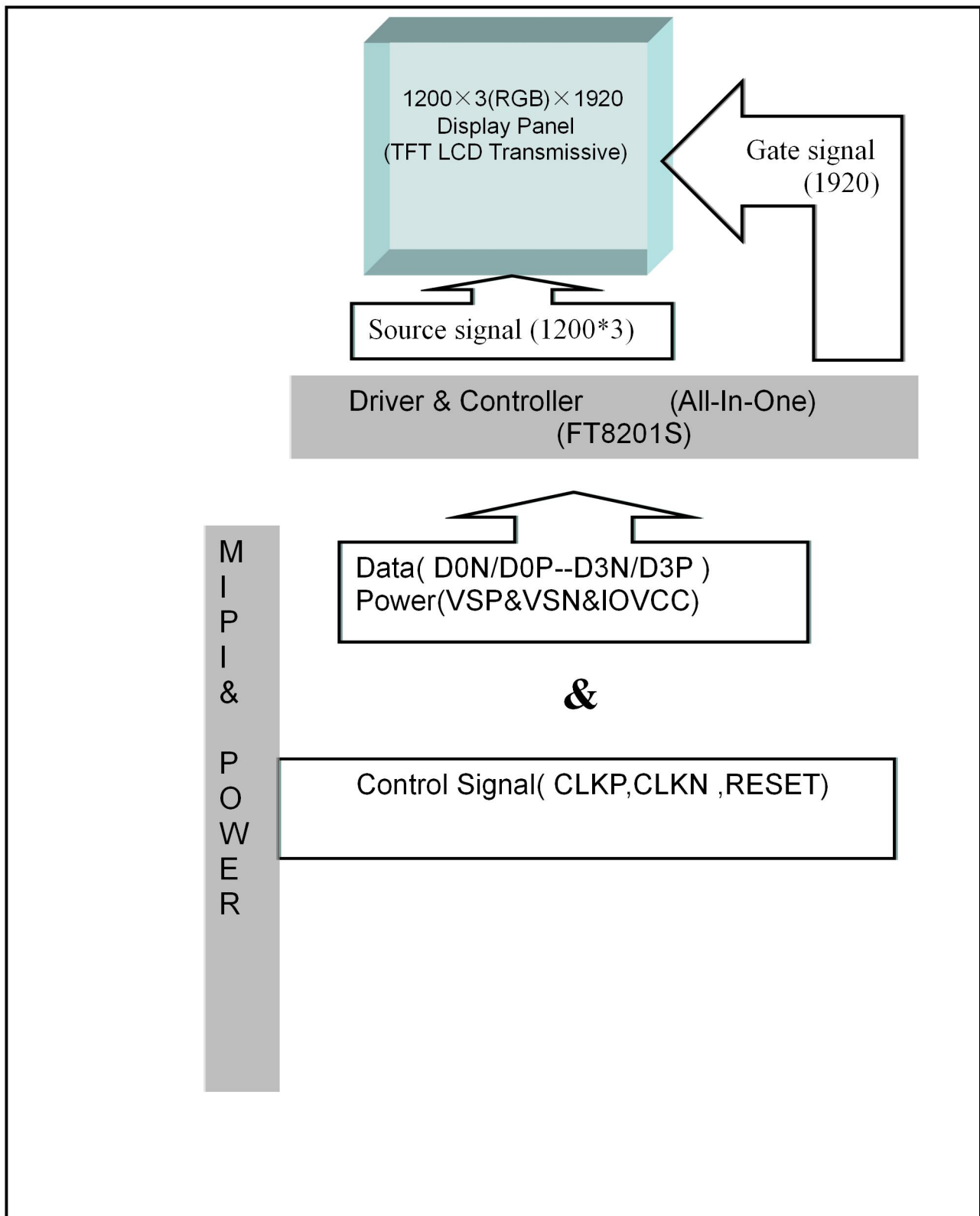


FIG. 3 The definition of Viewing Angle

Use Fig. 1(Test Procedure) under Measurement System to measure the contrast from the measuring direction specified by the conditions as the following figure.



4.4 Block Diagram



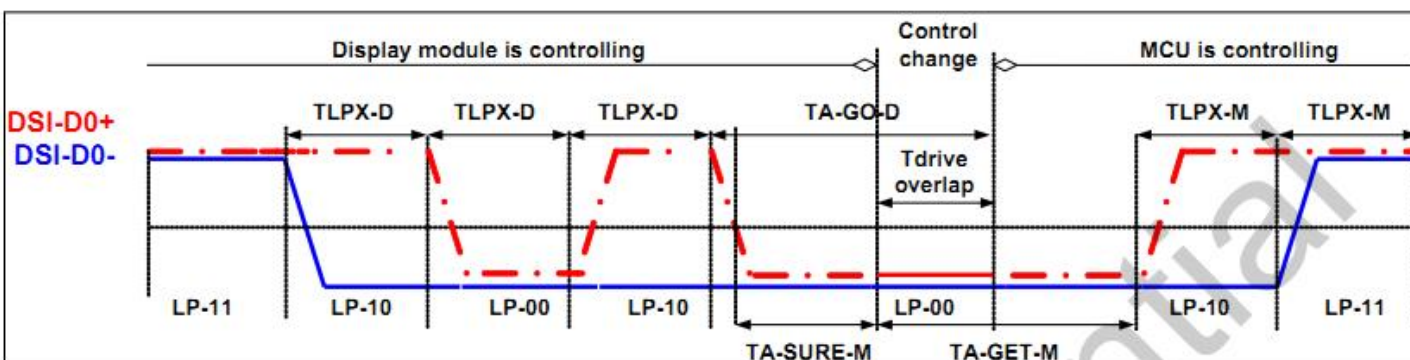
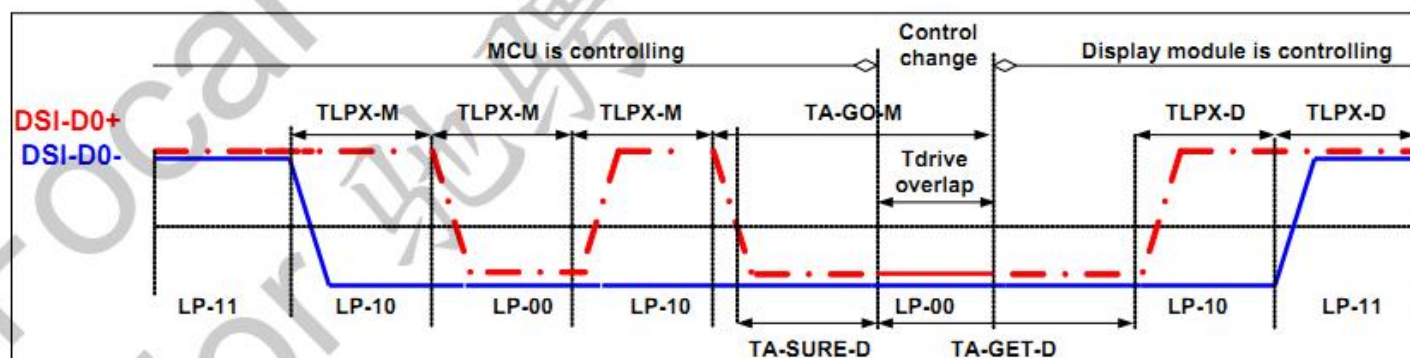
4.5 Pin Description

Item	Terminal	Functions
1-2	LEDA	B/L Power input PIN anode
3-4	NC	NC
5-6	LED-	B/L Power input PIN negative
7-8	NC	NC
9	GND	Ground
10	D0P_M	Positive polarity of low voltage differential data0 signal
11	D0N_M	Negative polarity of low voltage differential data0 signal
12	GND	Ground
13	D1P_M	Positive polarity of low voltage differential data1 signal
14	D1N_M	Negative polarity of low voltage differential data1 signal
15	GND	Ground
16	CLKP_M	positive polarity of low voltage differential clock signal
17	CLKN_M	Negative polarity of low voltage differential clock signal
18	GND	Ground
19	D2P_M	Positive polarity of low voltage differential data2 signal
20	D2N_M	Negative polarity of low voltage differential data2 signal
21	GND	Ground
22	D3P_M	Positive polarity of low voltage differential data3 signal
23	D3N_M	Negative polarity of low voltage differential data3 signal
24-25	GND	Ground
26-28	VSP	Positive power supply 5.8V
29-30	NC	NC
31-33	VSN	Negative power supply -5.8V
34-35	GND	Ground
36	ID0	NC
37	VDD	NC
38	PWM	NC
39	TE	Tear effect output
40-41	IOVCC	I/O Power supply 1.8V
42	RESET	LCD Reset, High=1.8V
43	GND	Ground
44	TP-RESET	IIC Reset, High=1.8V
45	TP-INT	IIC Interrupt
46	TP-SDA	IIC Interface data
47	TP-SCL	IIC Interface clock
48	TP-SPI_SS	NC
49	TP-SPI_SCL	NC
50	TP-SPI-MISO	NC
51	TP-SPI-MOSI	NC

4.6 Timing Characteristics

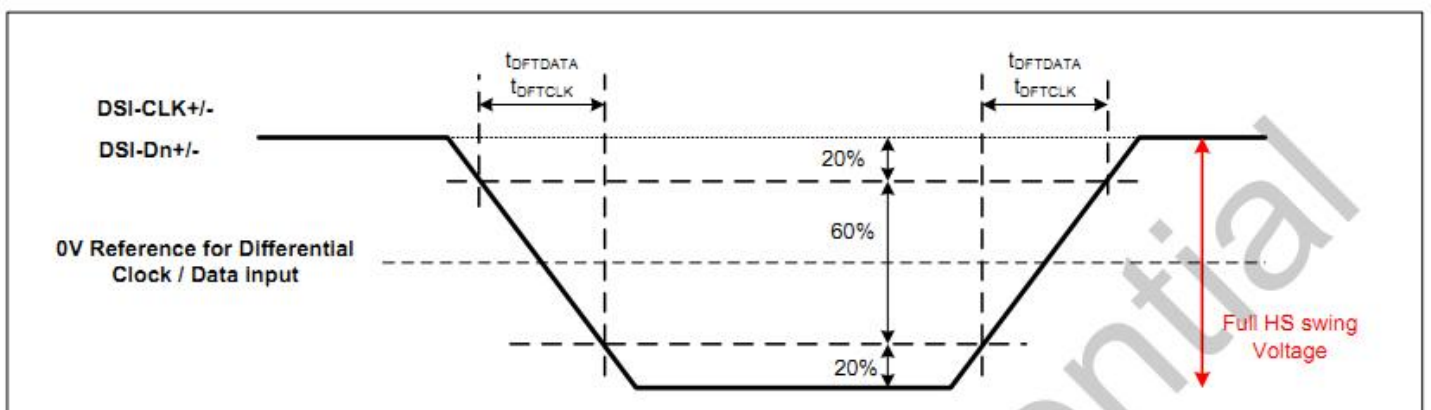
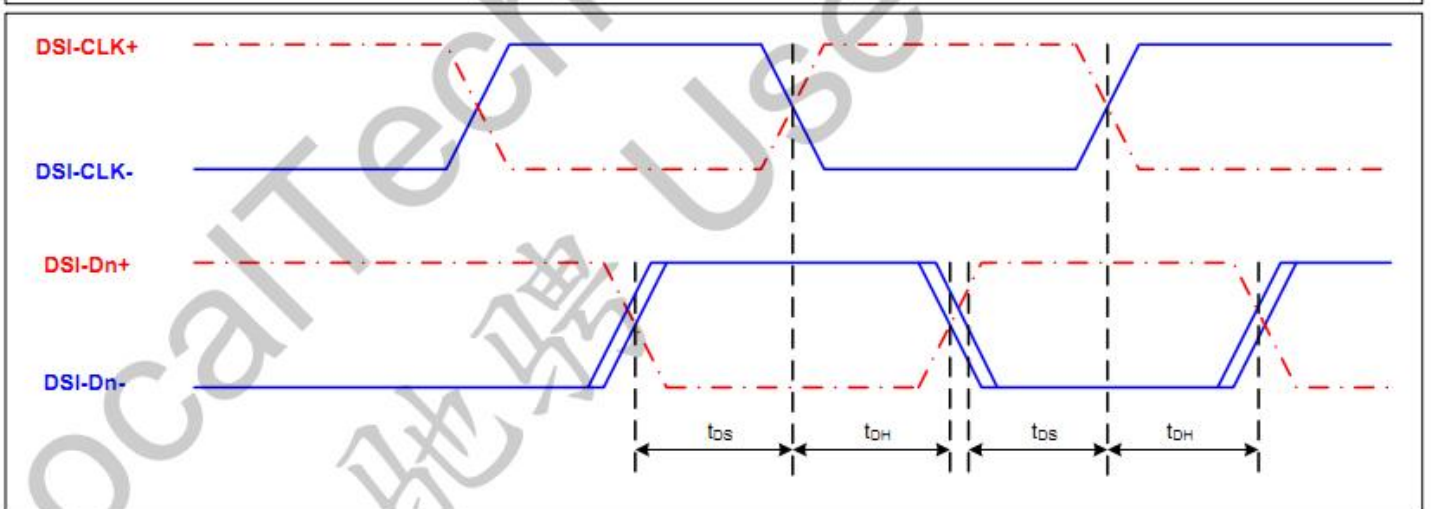
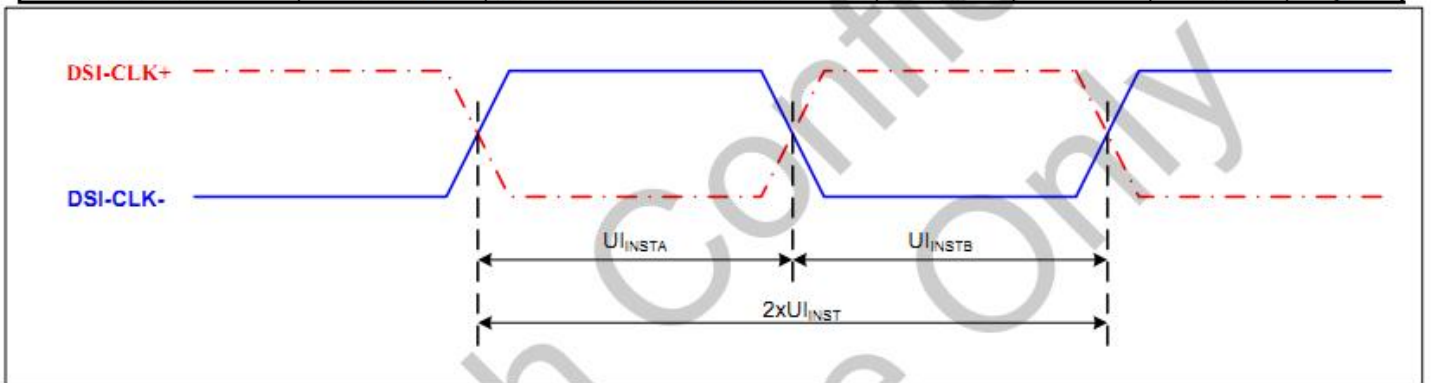
4.6.1 LP Power Mode Transmission

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Low Power mode						
DSI-D0+/-	T_{LPIX-M}	Transmitted length of any Low-Power state period (MCU)	50	-	-	ns
DSI-D0+/-	$T_{TA-SURE-M}$	The display module waits after the LP-10 before transmitting the LP-00 (MCU)	T_{LPIX-M}	-	$2XT_{LPIX-M}$	ns
DSI-D0+/-	$T_{TA-GET-M}$	The display module drives the LP-00 before releasing MCU control	$5XT_{LPIX-M}$	-	-	ns
DSI-D0+/-	$T_{TA-GO-M}$	The display drives the LP-00 after accepting control	$4XT_{LPIX-M}$	-	-	ns
DSI-D0+/-	Ratio T_{LPIX}	Ratio of (T_{LPIX-M}/T_{LPIX-D}) for driving overlap	2/3	-	3/2	-
DSI-D0+/-	T_{LPIX-D}	Transmitted length of any Low-Power state period (Display)	50	58	-	ns
DSI-D0+/-	$T_{TA-SURE-D}$	The MCU waits after the LP-10 before transmitting the LP-00 (Display)	T_{LPIX-D}	-	$2XT_{LPIX-D}$	ns
DSI-D0+/-	$T_{TA-GET-D}$	The MCU drives the LP-00 before releasing Display control	$5XT_{LPIX-D}$	-	-	ns
DSI-D0+/-	$T_{TA-GO-D}$	The MCU drives the LP-00 after accepting control	$4XT_{LPIX-D}$	-	-	ns



4.6.2 High Speed Mode Transmission

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Mode						
DSI-CLK+/-	2xUI _{INST}	Double UI instantaneous	1.54	-	25	ns
DSI-CLK+/-	UI _{INSTA} + UI _{INSTB}	UI instantaneous Halfs	0.77	-	12.5	ns
DSI-Dn+/-	t _{DS}	Data to clock setup time	0.15	-	-	UI
DSI-Dn+/-	t _{DH}	Data to clock hold time	0.15	-	-	UI
DSI-CLK+/-	t _{DRTCLK}	Differential rise time for clock	150	-	0.3UI	ps
DSI-Dn+/-	t _{DRTDATA}	Differential rise time for data	150	-	0.3UI	ps
DSI-CLK+/-	t _{DFTCLK}	Differential fall time for clock	150	-	0.3UI	ps
DSI-Dn+/-	t _{DFTDATA}	Differential fall time for data	150	-	0.3UI	ps



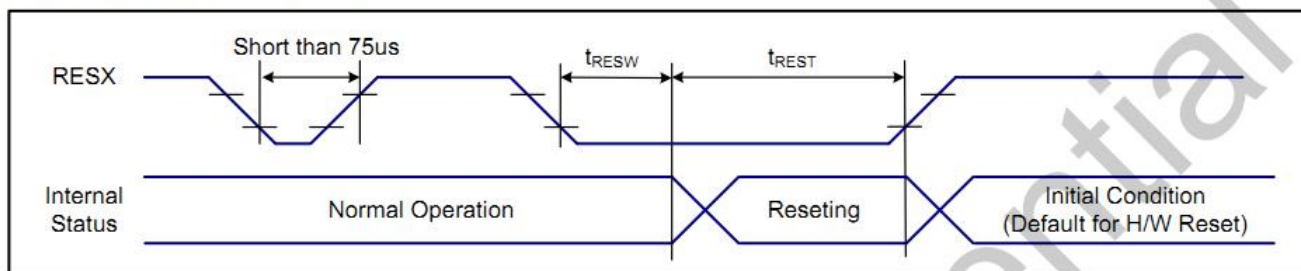
4.6.3 MIPI DC Character

(1a = -50°C ~ 85°C)

Parameter	Symbol	Conditions	Specification			Unit
			MIN	TYP	MAX	
Power supply voltage for MIPI Interface						
Power supply voltage for MIPI interface	LVDSVDD	-	1.2	1.25	1.3	V
LPDT Input Characteristics						
Pad signal voltage range	V _I	-	-50	-	1350	mV
Ground Shift	V _{GNDSH}	-	-50	-	50	mV
Logic 0 input threshold	V _{IL}	-	-	-	550	mV
Logic 1 input threshold	V _{IH}	-	880	-		mV
Input hysteresis	V _{HYST}	-	25	-	-	mV
LPDT Output Characteristics						
Output low level	V _{OL}	-	-50	-	50	mV
Output high level	V _{OH}	Note 1	1.2	1.25	1.3	V
Logic 0 contention threshold	V _{ILCD}	-	-	-	200	mV
Logic 1 contention threshold	V _{IHCD}	-	450	-	-	mV
Output impedance of LPDT	Z _{OLP}	-	110	-	-	Ω
Hi-speed Input Characteristics						
Single-end input low voltage	V _{ILHS}	-	-40	-	-	mV
Single-end input high voltage	V _{IHHS}	-	-	-	460	mV
Single-end threshold for HS termination enable	V _{TERM-EN}	-	-	-	450	mV
Differential input low threshold	V _{IDTL}	-	-70	-	-	mV
Differential input high threshold	V _{IDTH}	-	-	-	70	mV
Common mode voltage	V _{CMRXDC}	-	70	-	330	mV
Differential input impedance	Z _{ID}	-	80	100	125	Ω

4.6.4 Reset Operation

t_{RESW} shorter than 75us, Reset will be rejected.



$V_{SS}=0V$, $V_{DD1} = 1.65V \sim 1.95V$, $T_a = -30^{\circ}C$ to $85^{\circ}C$

Symbol	Parameter	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse minimum width	150	-	-	Reset signal recognized	us
t_{REST}	*2) Reset complete time	5	-	120	Reset action complete	ms

Table: Reset input timing

Note 1. RESX low pulse that is too short does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 75us	Reset Rejected
Longer than 150us	Reset Recognized
Between 75us and 150us	Reset sequence starts (It depends on voltage and temperature condition.)

Note 2. Once Reset low pulse is recognized, system requires RESX remaining low for another 5ms to complete H/W reset.

Note 3. During H/W Reset flow, ID0 ~ ID4 and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when H/W reset is complete ; The H/W reset sequence is complete when RESX is remaining low longer than $t_{RESW} + t_{REST}$.

5 Touch Description

5.1 Features and General Specification

Item	Contents	Unit
Cover Glass	0.7mm	
Size	13.4''	Inch
Outline of Cover Lens	197.22*305.11±0.1	mm
Cover Lens VA	180.42*288.31±0.15	mm
Transmittance	≥85%	
Surface treatment	AF	
Surface Hardness	≥6H	

5.2 IIC interface Characteristics

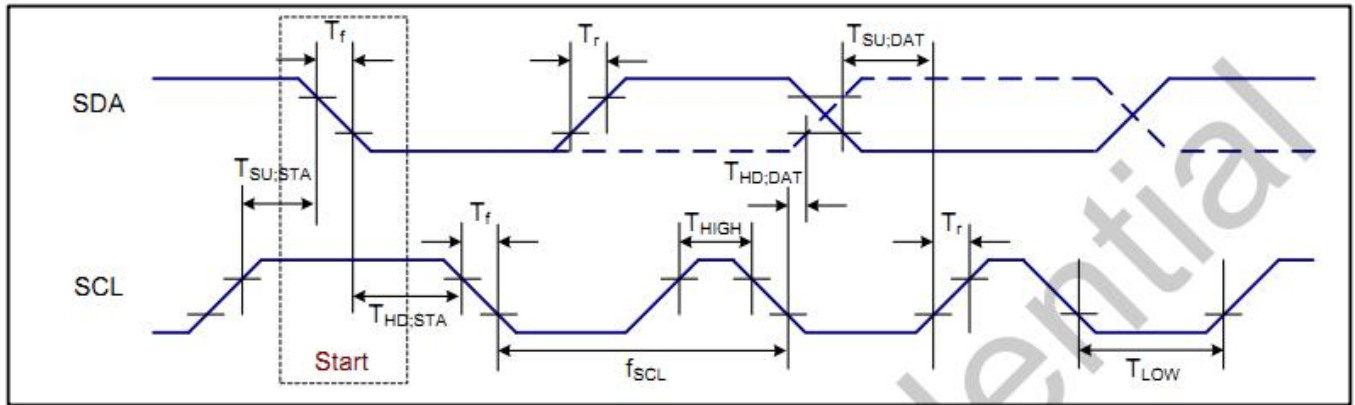


Table: I2C Interface Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{SCLK}	SCL clock frequency	-	10	-	400	kHz
T_{LOW}	SCL clock LOW period	-	1.2	-	-	us
T_{HIGH}	SCL clock HIGH period	-	0.6	-	-	us
$T_{SU:DATA}$	data set-up time	-	250	-	-	ns
$T_{HD:DATA}$	data hold time	-	0	-	0.9	us
T_r	SCL and SDA rise time	Note 2	$20+0.1C_b$	-	300	ns
T_f	SCL and SDA fall time	Note 2	$20+0.1C_b$	-	300	ns
T_f	SDA fall time for read out	-	$20+0.1C_b$	-	1000	ns
C_b	Capacitive load represented by each bus line	-	-	-	400	pF
$T_{SU:STA}$	Setup time for a repeated START condition	-	0.6	-	-	us
$T_{HD:STA}$	START condition hold time	-	0.6	-	-	us
$T_{SU:STO}$	Setup time for STOP condition	-	0.6	-	-	us
T_{SW}	Tolerable spike width on bus	Note 1	-	-	50	ns
T_{BUF}	BUS free time between a STOP and START condition	-	4.7	-	-	us

Note1: The device inputs SDA and SCL are filtered and will reject spikes on the bus lines of width $< t_{sw(max)}$.

Note2: The rise and fall times specified here refer to the driver device and are part of the general fast I²C-bus specification. C_b = capacitive load per bus line.

Note3: All timing values are valid within the operating supply voltage and ambient temperature ranges and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DDI} .