

#### Manufacturer Certificated





CERT. No.: 282Q19070712006

CERT. No.: 282E19070712007

# **Product Specification**

Model: <u>TTW128128D-A0</u> 128X128 COG Module

This module uses RoHS material



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# **Specification Revision History**

Version	Content	Date
A0	First Issue	27-Apr-18

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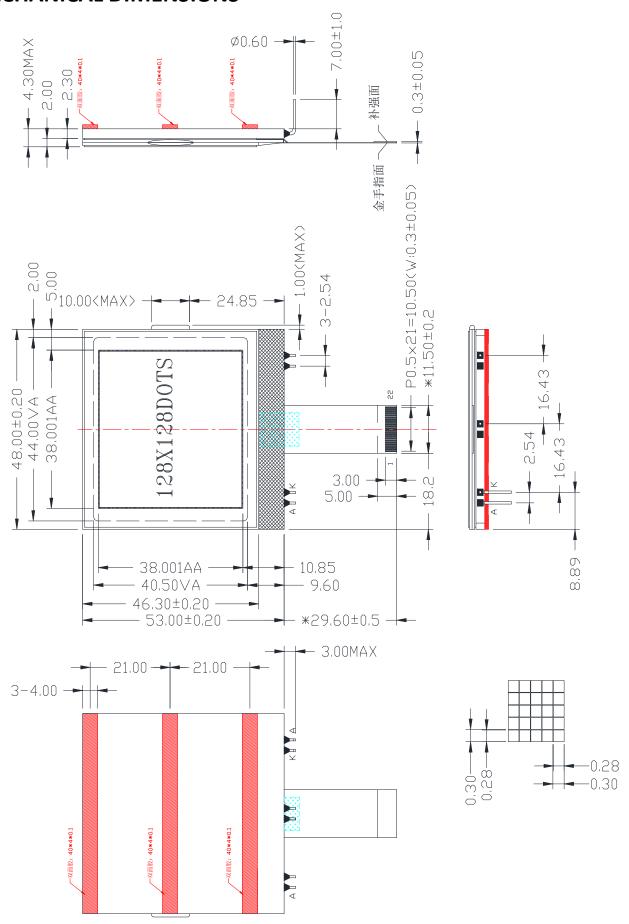


# **■** GENERAL SPECIFICATIONS

ITEM	STANDARD VALUE	UNIT
NUMBER OF GRAPHIC	128×128	
MODULE DIMENSION	48.0×53.0×12.3(MAX)	mm
EFFECTIVE DISPLAY AREA	44.0×40.5	mm
DOT SIZE	0.282×0.282	mm
DOT PITCH	0.297×0.297	mm
LCD TYPE	FSTN/POSITIVE/TRANSFLECTIVE	
DUTY	1/128duty 1/11bias	
VIEWING DIRECTION	6	o'clock
POLARIZING FILM HAZE	(防眩目)25	%
OPERATING TEMPERATURE	-10~+50	$^{\circ}$
STORAGE TEMPERATURE	-30~+80	$^{\circ}$
BACK LIGHT TYPE	SIDE LED	
BACK LIGHT COLOR	WHITE	
APPROX. WEIGHT	60	g
ROHS STANDARD	YES	_



# ■ MECHANICAL DIMENSIONS





# ■ INTERFACE PIN CONNECTIONS

VLCD	PIN	SYMBOL	FUNCTIONS				
SEG driving currents. These voltages are generated internally. Connect capacitors of CBXvalue between VBX+ VBO+ VBX	1	VLCD	High volta	ge LCD	Power Su	pply.	
The internal of the internal of the color	2	VB0-	LCD Bias V	oltages	. These	are the volta	age sources to provide
The interface bus mode is determined by BM[1:0] and Different following relationship:	3	VB1-	SEG drivin	g curre	nts. The	se voltages	are generated
Bus mode: The interface bus mode is determined by BM[1:0] and Dithe following relationship:	6	VB1+	internally	. Conne	ct capac	itors of CBX	value between VBX+and
## BM1   BM1   BM1   Data   G800/8-bit	7		-				
BM1						node is determi	ned by BM[1:0] and D[7:6] b
11	4	RW1	1	1	isnip.	Mode	
10	-	DILL					
5   BMO			1				
5   BMO			01	11		2-wire I <sup>2</sup> C	
8 VDD power supply 9 VSS Power Ground. 10 WR1 WR\[1:0] controls the read/write operation of the 11 WR0 hostinterface. See section HostInterfaceformoredetail. I Select Control data or Display data for read/write oper 12 CD In I2C mode, CD pin is not used. Connect CD to VSS when used. "L" ±: Control data "H" ±: Display data 13 CSO Chip Select. Chip is selected when CSO = "L" When RST="L" ±, all control registers are 14 RST re-initialized by their default states.  Bi-directional bus for both serial and parallel host interfaces. In serial modes, connect D[0] to SCK, D[3] to SDA,  BM=1x (Parallel) (PC) (S8/S8uc) D0 D0 SCK SCK D1 D1 D1 D1 D1 SDA D3 D3 SDA SDA D4 D4 D4 D4 D5 D5 D5 DA D6 D6 D6 SCK SCK D7 D6 D7	-	PMO			4-wire	SPI w/ 8-bit toke	en
9 VSS Power Ground. 10 WR1 WR\[1:0] controls the read/write operation of the 11 WR0 hostinterface. See section HostInterfaceformoredetail. I  Select Control data or Display data for read/write oper 12 CD In I2C mode, CD pin is not used. Connect CD to VSS when used. "L" ±: Control data "H" ±: Display data 13 CSO Chip Select. Chip is selected when CSO = "L"  When RST="L" ±, all control registers are 14 RST re-initialized by their default states.  Bi-directional bus for both serial and parallel host interfaces. In serial modes, connect D[0] to SCK, D[3] to SDA,  BM=1x BM=01 BM=00 (Parallel)	5	DMU	00	11	3-wire	SPI w/ 8-bit toke	
10 WR1 WR\[1:0] controls the read/write operation of the 11 WR0 hostinterface. See section HostInterfaceformoredetail. I  Select Control data or Display data for read/write oper 12 CD In I2C mode, CD pin is not used. Connect CD to VSS when used. "L" ±: Control data "H" ±: Display data 13 CSO Chip Select. Chip is selected when CSO = "L"  When RST="L" ±, all control registers are 14 RST re-initialized by their default states.  Bi-directional bus for both serial and parallel host interfaces. In serial modes, connect D[0] to SCK, D[3] to SDA,  BM=1x (Parallel) (PC) (SB/SBUC)  DO DO SCK SCK  DO SCK SCK  DO DO SCK SCK  DO	8	VDD	power supp	ly			
11 WRO hostinterface. See section HostInterfaceformoredetail. It Select Control data or Display data for read/write oper 12 CD In I2C mode, CD pin is not used. Connect CD to VSS when used. "L" ±: Control data "H" ±: Display data 13 CSO Chip Select. Chip is selected when CSO = "L" When RST="L" ±, all control registers are 14 RST re-initialized by their default states.    Bi-directional bus for both serial and parallel host interfaces. In serial modes, connect D[0] to SCK, D[3] to SDA,     BM=1x   BM=01   (Parallel)   (Pa	9	VSS	Power Grou	nd.			
11 WRO hostinterface. See section HostInterfaceformoredetail. It Select Control data or Display data for read/write oper 12 CD In I2C mode, CD pin is not used. Connect CD to VSS when used. "L" ±: Control data "H" ±: Display data 13 CSO Chip Select. Chip is selected when CSO = "L" When RST="L" ±, all control registers are 14 RST re-initialized by their default states.    Bi-directional bus for both serial and parallel host interfaces. In serial modes, connect D[0] to SCK, D[3] to SDA,   BM=1x BM=01 (Parallel) (Pa	10	WR1	WR\[1:0] c	ontrols	the rea	d/write opera	ation of the
In I2C mode, CD pin is not used. Connect CD to VSS when used. "L" ±: Control data "H" ±: Display data  CSO Chip Select. Chip is selected when CSO = "L"  When RST="L" ±, all control registers are  re-initialized by their default states.  Bi-directional bus for both serial and parallel host interfaces. In serial modes, connect D[0] to SCK, D[3] to SDA,  BM=1x BM=01 BM=00 (Parallel) (Parallel) (Parallel) (S8/S8uc)  DO DO SCK SCK  DO DO SCK SCK DO DO SCK SCK DO DO SCK SCK DO DO SCK SCK DO DO SCK SCK DO DO SCK SCK DO DO SCK SCK DO DO SCK SCK DO DO SCK SCK DO S	11	WRO				The second second second second	
13   CSO   Chip Select. Chip is selected when   CSO = "L"   When RST="L" ± , all control registers are     14   RST   re-initialized by their default states.	12	CD	In I2C mod	le, CD p	in is no	t used. Conn	ect CD to VSS when not
When RST="L" ± , all control registers are re-initialized by their default states.    Bi-directional bus for both serial and parallel host interfaces.	13	CSO					
14 RST re-initialized by their default states.  Bi-directional bus for both serial and parallel host interfaces.  In serial modes, connect D[0] to SCK, D[3] to SDA,    BM=1x   BM=01   BM=00     (Parallel)   (I^2C)   (S8/S8uc)     D0   D0   SCK   SCK     D1   D1   -   -     D2   D2   -   -     D3   D3   SDA   SDA     D4   D4   -   -     D5   D5   -   -							
In serial modes, connect D[0] to SCK, D[3] to SDA,    BM=1x   BM=01   BM=00     (Parallel)   (I^2C)   (S8/S8uc)     D0   D0   SCK   SCK     D1   D1   -   -     D2   D2   D -   -     D3   D3   SDA   SDA     D4   D4   -   -     D5   D5   -   -	14	RST					
15~22 D7~D0   CParallel) (I²C) (S8/S8uc)   D0						A STATE OF THE PARTY OF THE PAR	erfaces.
15~22 D7~D0 D0 SCK SCK SCK D1 D1 D1				and the second s			
15~22 D7~D0 D1 D1 D2 D2 D3 D3 D3 D4 D4 D4 D5 D5 D5 D5 D5 D5							
15 22 D7 D0 D2 D2 — — — — — — — — — — — — — — — — —	~-	~			-	-	
D3 D3 SDA SDA D4 D4 — — D5 D5 — —	15 22	D7 D0			-	-	
D5 D5			D3	D3	SDA	SDA	
The state of the s			7		-	_	
DC DC 4 C0/C0va					7		
			D6	D6	1	S8/S8uc	
D7 D7 1 1  Connect unused pins to V <sub>SS</sub> .						1	



### ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply voltage for logic	VDD	-0.3	4.0	V
Supply voltage for LCD	VEE-VSS	-0.3	+19.8	V
Input voltage	VI	-0.3	VDD+0.5	V
Output voltage	Vo	-0.3	VDD+0.5	V
Operating temperature	TOP	-10	+50	٥°
Storage temperature	TST	-30	+80	°C

### ■ ELECTRICAL CHARACTERISTICS

#### **▼** DC Characteristics

Condition: VDD=+3.3V±10%, VSS=0V, VEE-VSS=0 to 18V, Ta=-30 to +85  $^{\circ}$ C

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Supply voltage for logic	VDD		2.7	3.3	3.5	V
Supply current for logic	IDD			2.0	2.5	mA
Operating voltage for LCD	VLCD-VSS		9.8	10.0		٧
Input voltage ' H ' level	Vih		0.8VDD		VDD	V
Input voltage ' L ' level	VIL		VSS		0.2VDD	V

#### AC Characteristics

System Bus Read/Write Characteristics (For the 8080 Series MPU) VDD=+3.3V±10%, VSS=0V, Ta=-30 to +85 °C

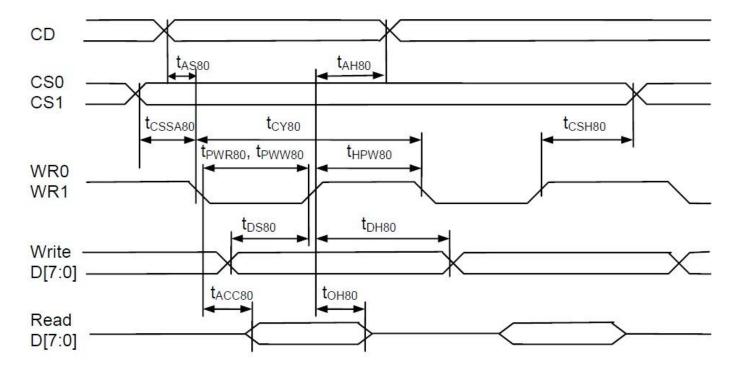


FIGURE 13: Parallel Bus Timing Characteristics (for 8080 MCU)



 $(2.5V \le V_{DD} \le 3.3V$ , Ta= –30 to +85 $^{\circ}$ C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t <sub>AS80</sub> t <sub>AH80</sub>	CD	Address setup time Address hold time		0	-	nS
t <sub>CY80</sub>		System cycle time (read) (write)		170 130	-	nS
t <sub>PWR80</sub>	WR1	Pulse width (read)		85	-	nS
t <sub>PWW80</sub>	WR0	Pulse width (write)		65	_	nS
t <sub>HPW80</sub>	WR0, WR1	High pulse width (read) (write)		85 65	-	nS
t <sub>DS80</sub> t <sub>DH80</sub>	D0~D7	Data setup time Data hold time		30 0	1	nS
t <sub>ACC80</sub> t <sub>OH80</sub>		Read access time Output disable time	C <sub>L</sub> = 100pF	-	65 30	nS
t <sub>CSSA80</sub> t <sub>CSH80</sub>	CS1/CS0	Chip select setup time Chip select hold time		5 5		nS

System Bus Read/Write Characteristics (For the 6800 Series MPU) VDD=+3.3V $\pm$ 10%, VSS=0V, Ta=-30 to +85  $^{\circ}$ C

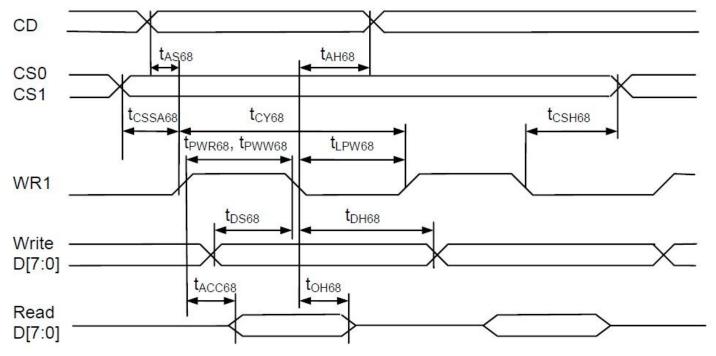


FIGURE 14: Parallel Bus Timing Characteristics (for 6800 MCU)



 $(2.5V \le V_{DD} \le 3.3V$ , Ta= -30 to +85 $^{\circ}$ C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t <sub>AS68</sub> t <sub>AH68</sub>	CD	Address setup time Address hold time		0	1	nS
t <sub>CY68</sub>		System cycle time (read) (write)		170 130	-	nS
t <sub>PWR68</sub>	WR1	Pulse width (read)		85	_	nS
t <sub>PWW68</sub>		Pulse width (write)		65	_	nS
t <sub>LPW68</sub>		Low pulse width (read) (write)		85 65	-	nS
t <sub>DS68</sub> t <sub>DH68</sub>	D0~D7	Data setup time Data hold time		30 0	-	nS
t <sub>ACC68</sub> t <sub>OH68</sub>		Read access time Output disable time	C <sub>L</sub> = 100pF	-	70 30	nS
tcssa68 t <sub>csh68</sub>	CS1/CS0	Chip select setup time Chip select hold time		5 5		nS

System Bus Read/Write Characteristics (For the S8 / S8uc Series MPU) VDD=+3.3V±10%, VSS=0V, Ta=-30 to +85 ℃

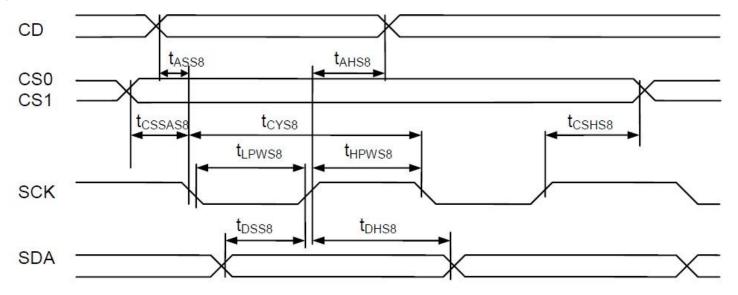


FIGURE 15: Serial Bus Timing Characteristics (for S8 / S8uc)

 $(2.5V \le V_{DD} \le 3.3V$ , Ta= –30 to +85 $^{\circ}$ C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t <sub>ASS8</sub>	CD	Address setup time		0	_	nS
t <sub>AHS8</sub>	CD	Address hold time		0	_	nS
t <sub>CYS8</sub>		System cycle time		40	_	nS
t <sub>LPWS8</sub>	SCK	Low pulse width		20	-	nS
t <sub>HPWS8</sub>		High pulse width		20	_	nS
t <sub>DSS8</sub> t <sub>DHS8</sub>	SDA	Data setup time Data disable time		15 0	_	nS
tcssas8 t <sub>CSHS8</sub>	CS1/CS0	Chip select setup time Chip select hold time		5 5		nS



System Bus Read/Write Characteristics (For the I2C Series MPU) VDD=+3.3V $\pm$ 10%, VSS=0V, Ta=-30 to +85  $^{\circ}$ C

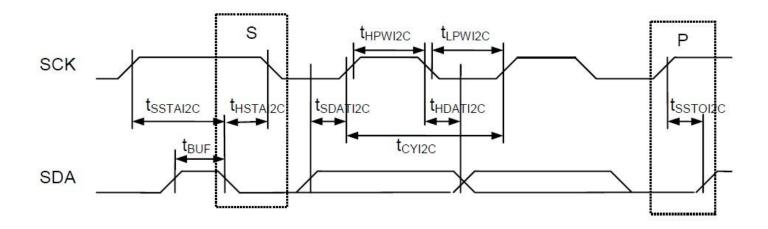


FIGURE 16: Serial bus timing characteristics (for I<sup>2</sup>C)

 $(2.5V \le V_{DD} \le 3.3V$ , Ta= –30 to +85 $^{\circ}$ C)

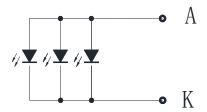
Symbol	Signal	Description	Condition	Min.	Max.	Units
t <sub>CYI2C</sub>		SCK cycle time (read) (write)	tr+tf ≤ 100nS	580 275	1	nS
t <sub>LPWI2C</sub>	SCK	Low pulse width (read) (write)		290 165	1	nS
t <sub>HPWI2C</sub>		High pulse width (read) (write)		290 110	-	nS
tr, tf		Rise time and fall time		-	-	nS
t <sub>SSDAI2C</sub>		Data setup time		28	_	nS
t <sub>HDAI2C</sub>		Data hold time		11	-	nS
t <sub>SSTAI2C</sub>	SCK	START Setup time		28	_	nS
t <sub>HSTAI2C</sub>	SDA	START Hold time		28	_	nS
t <sub>SSTOI2C</sub>	1	STOP setup time		28	_	nS
T <sub>BUF</sub>		Bus Free time between STOP and START condition		165	1	nS

### ■ BACKLIGHT

### **▼** Backlight Type

Backlight Type: LED Backlight color: white

### **▼** Power Supply For Backlight



# Absolute Maximum Rating

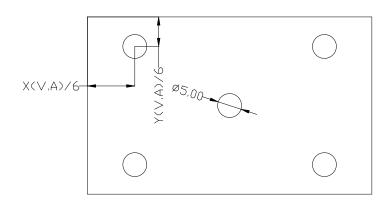
PARAMETER	SYMBOL	CONDITION	MAX	UNIT
Absolute maximum forward current	Ifm		60	mA
Peak forward current	Ifp	1 MSEC plus 10% Duty Cycle	120	mA
Reverse voltage	VR		7.0	V
Life	Hour	If(forward current) =45mA	80000	Н

Note: For operation above  $25^{\circ}$ C, Then Ifm Ifp must be decreased, the Current decreased is -1.08mA/°C for DC drive and -2.58mA/°C Pulse drive, the power dissipation is -4.5mW/°C. The product working current must not more than the 70% of the Ifm or Ifp according to the working temperature.

# **▼** Electrical-Optical Characteristics

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Forward voltage	Vf		2.7	3.3	3.5	V
Forward voitage	(LED(+)-LED(-))		2.7	3.3	3.3	V
Forward current	If			45	60	mA
Reverse current	lr	VR=7.0V			120	μΑ
Chromaticity	) n	If(forward current) = 45mA	x=0.28	x=0.30	x=0.32	
Chromaticity	λр	ii(iorward current) = 45iiiA	y=0.27	y=0.29	y=0.31	
Luminance	Lv	If(forward current) =45mA	200			$cd/m^2$

Note:The Master Screen's luminance is the average value of 5 points, and The Lymin./Lymax. is not less than 70%. The measurement instrument is BM-7 luminance Colorimeter. The aperture is Ф5 mm.





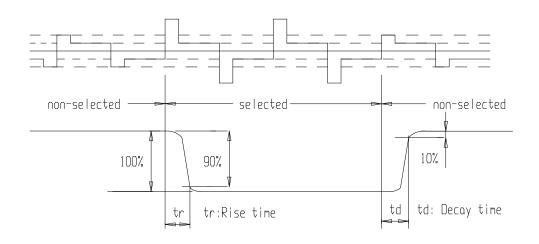
#### OPTICAL CHARACTERISTICS

Test instrument is LCD-5000, made in Japan

Item	Symbol	Condition	Min	Тур	Max	Unit	Remarks	Note
Operating voltage	Vop	<b>25</b> ℃		TBD		V		
Posnonso timo	Tr			350	400	ms		1
Response time	Td			380	400	ms		1
Contrast ratio	Cr			24				2
Viewing angle	0	C*>6		60		deg	<b>Ø</b> =0 °	3
range	θ	Cr≥6		28		deg	Ø=180°	3

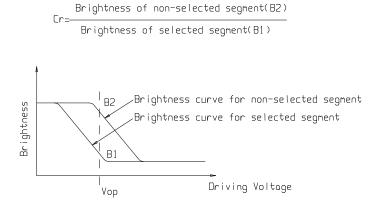
# Definition Of Viewing Angle

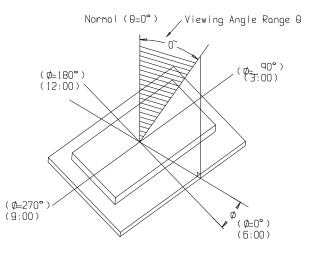
Note1: Definition of response time



Note2: Definition of contrast ratio 'Cr'

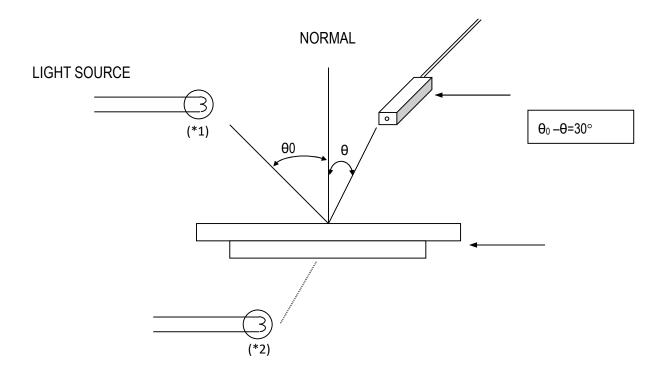
Note3: Definition of viewing angle range ' $\theta$ '







# Note4:Measuring Instruments For Electro-optical Characteristics



- \*1.Light source position for measuring the reflective type of LCD panel
- \*2.Light source position for measuring the transflective / transmissive types of LCD panel



# ■ OPERATING PRINCIPLES & METHODS

# **▼** Control registers

Name	Bits	Default	Description									
SL	7	0H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value is between 0 (no scrolling) and (127– 2x(FLT+FLB)). Setting SL outside of this range causes undefined effect on the displayed image.									
FLT FLB	4	0H 0H	Fixed Lines. The first FLTx2 lines and the last FLBx2 lines (relative to CEN) of each frame are fixed and are not affected by scrolling (SL).									
			When FLT and/or FLB are non-zero, the screen is effectively separated into three regions: one scrollable, surrounded by two non-scrollable regions.									
			When partial display mode is activated, the display of these 2xFLT and 2xFLB lines is also controlled by LC[0]. When LC[0]=1, the display will have three sections, 2xFLT on one side non-scrollable, 2XFLB on the other side also non-scrollable, and scrollable DST~DEN in the middle.									
CR	5	0H	Return Page_C Address. Useful for cursor implementation.									
CA	5	0H	Display Data RAM Page_C Address (Used in Host to Display Data RAM access)									
RA	7	0H	Display Data RAM Row Address (Used in Host to Display Data RAM access)									
BR	2	3H	Bias Ratio. The ratio between V <sub>LCD</sub> and V <sub>BIAS</sub> .  00b: 6 01b: 9  10b: 10 11b: 11									
TC	2	0H	Temperature Compensation (per °C)  00b: -0.00%									
PM	8	4EH	Electronic Potentiometer to fine tune V <sub>BIAS</sub> and V <sub>LCD</sub>									
РМО	6	-	PM offset. PMO[5] = 1: The effective PM value, PMV = PM – PMO[4:0] PMO[5] = 0: The effective PM value, PMV = PM + PMO[4:0]									
PC	4	EH	Power Control.									
			PC[1:0]: 00b: LCD: ≤ 6nF 01b: LCD: 6~9nF 10b: LCD: 9~13nF 11b: LCD: 13~18nF									
			PC[3:2]: 00b: External V <sub>LCD</sub> 11b: Internal V <sub>LCD</sub> (9X pump, standard)									
DC	4	8H	Display Control:  DC[0]: PXV: Pixels Inverse. Bit-wise data inversion. (Default 0: OFF)  DC[1]: APO: All Pixels ON (Default 0: OFF)  DC[2]: Display ON/OFF (Default 0: OFF)  DC[3]: Gray Shade and B/W mode  0b: B/W Mode  1b: 4-Shade Mode									



# **▼** Command table

C/D: 0: Control, 1: Data W/R: 0: Write Cycle, 1: Read Cycle # Useful Data bits – Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3	Get Status		1		MX er	MY	WA	DE	WS (5:0)	MD	MS	Get (Status, Ver, PMO, Product Code,	N/A
				Product Code			e	_	ID		ID	PID, MID}	
4	Set Page_C Address	0	0	0	0	0	#	#	#	#	#	Set CA[4:0]	OH
5	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	00b
6	Set Panel Loading	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	10b
7	Set Pump Control	0	0	0	0	1	0	11	1	#	#	Set PC[3:2]	11b
8	Set Adv. Program Control (double-byte command)	0	0	0 #	0 #	1 #	1 #	0	0 #	R #	R #	Set APC[R][7:0], R = 0, 1 or 2	N/A
M	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	OH
9	Set Scroll Line MSB	0	0	0	1	0	1	The "	#	#	#	Set SL[6:4]	OH
	Set Row Address LSB	0	0	0	1	1	0	#	#	#	#	Set RA[3:0]	00H
10	Set Row Address MSB	0	0	0	1	1	1	120	#	#	#	Set RA[6:4]	00H
11	Set V <sub>BIAS</sub> Potentiometer (double-byte command)	0	0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	Set PM[7:0]	4EH
12	Set Partial Display Control	0	0	1	0	0	0	0	1	#	#	Set LC[9:8]	00b: Disable
13	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
14	Set Fixed Lines	0	0	1 #	0 #	0 #	1 #	0 #	0 #	0 #	0 #	Set {FLT, FLB}	0
15	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	00b
16	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0b
17	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0b
18	Set Display Enable	0	0	1	0	1	0	1	1	#	#	Set DC[3:2]	10b
19	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	000b
20	Set N-Line Inversion	0	0	1	1	0	0	1 #	0 #	0 #	0 #	Set NIV[3:0]	6H
21	Set LCD Gray Shade	0	0	1	1	0	1	0	#	#	#	Set LC[7:5]	001b
22	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
23	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
24	Set Test Control (double-byte command)	0	0	1 #	1 #	1 #	0 #	0	1 #	#	T #	For testing only. Do not use.	N/A
25	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	11b: 11
	Reset Cursor Update Mode	0	0	1	1	1	0	1	1	1	0	AC[3]=0, CA=CR	AC[3]=0
27	Set Cursor Update Mode	0	0	1	1	1	0	1	1	1	1	AC[3]=1, CR=CA	AC[3]=1
28	Set COM End	0	0	1	1 #	1 #	1 #	0 #	0 #	0 #	1 #	Set CEN[6:0]	127
29	Set Partial Display Start	0	0	1	1 #	1 #	1 #	0 #	0 #	1 #	0 #	Set DST[6:0]	0
30	Set Partial Display End	0	0	1	1 #	1 #	1 #	0 #	0 #	1 #	1 #	Set DEN[6:0]	127

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Actio	n	Default
31	Set Window Program Starting Page_C Address	0	0	1	1	1	1 #	0 #	1 #	0	0 #		Set WPC0	0
32	Set Window Programming Starting Row Address	0	0	1	1 #	1 #	1 #	0	1 #	0 #	1 #	Shared with	Set WPP0	0
33	Set Window Programming Ending Page_C Address	0	0	1	1	1	1 #	0 #	1 #	1 #	0 #	MTP commands	Set WPC1	31
34	Set Window Programming Ending Row Address	0	0	1	1 #	1.	1 #	0 #	1 #	1 #	1 #		Set WPP1	127
35	Enable window program	0	0	1	1	1	1	1	0	0	#	Set AC[4]		0: Disable
36	Set MTP Operation control	0	0	1	0	1 #	1 #	1 #	0 #	0 #	0 #	Set MTPC[5:0]		10H
37	Set MTP Write Mask	0	0	1 #	0 #	1 #	1 #	1 #	0 #	0 #	1 #	Set MTPN	M[7:0]	0
38	Set V <sub>MTP1</sub> Potentiometer	0	0	1 #	1 #	1 #	1 #	0	1 #	0 #	0 #		Set MTP1	
39	Set V <sub>MTP2</sub> Potentiometer	0	0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	1 #	Shared with	Set MTP2	N/A
40	Set MTP Write Timer	0	0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	0 #	Window Program commands	Set MTP3	
41	Set MTP Read Timer	0	0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	1 #	commands	Set MTP4	

#### Notes:

- Any bit patterns other than the commands listed above may result in undefined behavior.
- The interpretation of commands (37)~(41) depends on register MTPC[3].
- Commands (38)~(41) are shared with commands (31)~(34) and have exactly the same code.
   When MTPC[3]=0, commands (38)~(41) are interpreted as Window Programming commands.
   When MTPC[3]=1, they are the MTP Control commands.
- MTPM and PM are actually the same register. Only one of the commands (37 or 11) is valid at any time, and it is determined by MTPC[3].
- After MTP-ERASE or MTP-PROGRAM operation, before resuming normal operation, please always a) Remove TST4 power source,
   b) Do a full V<sub>DD</sub> ON-OFF-ON cycle.



#### **▼** DDRAM

T 2	0/10	03/2	D5/4	9110	0710	03/2	790	8110	0110	780	190	9//0	MY	/-D	MY	<b>7-1</b>
-						11		400	-			-	SL-Q	SL-16	SL-0	SL-1
1			П			)=0			910	17	, F.	+1	R1	R113	R128	R16
					į.					Ш	2		R2	R114	R127	R15
							-		100	1			R3	R115	R126	R14
	$\vdash$	_						-			-		R4	R116	R125	R13
										1			R5	R117	R124	R12
	$\mathbf{L}$		0.0	$\Box$			-		_				R6	R118	R123	R11
	Н	-		ш	-	_			-		-		R7	R19	R122	R10
	1			ш							1	100	R8	R120	R121	R9
	-	-		Н		_	-	-	 -				R9	R121	R120	R8
	-	-		Н			-		-		1		R10	R122	R119	R7
	$\vdash$				$\vdash$	$\vdash$	-				-		R11	R123	R118	R6
	-						-	-				-	R12	R124 R125	R117	R5 R4
	-	-		Н	_	_	-	-	-			-	R13			R3
	-						-				-	_	R15	R126 R127	R115 R114	R2
	-	-		Н	-				+	-		-	R16	R128	R113	R1
	-						-		1		-	-	R17	R1	R112	R12
	Н	-				-		$\vdash$					R18	R2	R111	R12
				$\vdash$									R19	R3	R110	R12
							-					$\rightarrow$	R20	R4	R109	R12
	Н										-		R21	R5	R108	R12
			-				1						R22	R6	R107	R12
	_			Н					+		_		R23	R7	R106	R12
	-											-	R24	R8	R105	R12
										100			R25	R9	R104	R12
									1				R26	R10	R103	R11
	-								-		-					
	_	_											R27	R11	R102	D. 1.3
	Pat	ge C	0		Pad	ne C	1		Pac	e C	31		R28	R11	R102 R101	R118
	Pag	ge_C	0		Pag	ge_C	1		Pag	je_C	31					
	Pag	ge_C	0		Pag	ge_C	at .		Pag	pe_C	31					
	Pa	ge_C	:0		Pag	ge_C	1		Pag	e_C	31		R28	R12	R101	R11
	Pag	ge_c	0		Pag	ge_C	at		Pag	e_C	31		R28	R12	R101	R11
	Pag	ge_C	0		Pag	ge_C	1		Pag	e_C	31		R109 R110	R12 R93 R94	R101 R20 R19	R111
	Pag	ge_C	0		Pag	ge_C	at		Pag	e_C	31		R109 R110 R111 R112 R113	R12 R93 R94 R95	R101 R20 R19 R18	R111 R36 R35 R34
	Pay	ge_C	o d		Pag	ge_C	1		Pag	e_C	31		R109 R110 R111 R111 R113 R114	R93 R94 R95 R96 R96 R97 R98	R101 R20 R19 R18 R17 R16 R15	R36 R36 R35 R34 R33 R32 R31
	Pa	ge_C	20		Pag	ge_C	1		Pag	ne_C	31		R109 R110 R111 R112 R113 R114 R115	R12 R93 R94 R95 R96 R97 R98 R99	R1D1 R2D R19 R18 R17 R16 R15 R14	R36 R36 R35 R34 R33 R32 R31
	Pay	ge_C	:0		Pag	ge_C	at the second se		Pag	ne_C	:31		R109 R110 R111 R112 R113 R115 R116	R12 R93 R94 R95 R96 R97 R98 R99 R100	R1D1 R2D R19 R18 R17 R16 R15 R14 R13	R36 R36 R35 R34 R33 R32 R31 R30
	Pag	ge_C	:0		Pag	ge_C	21		Pag	ne_C	31		R109 R110 R111 R112 R113 R114 R116 R116	R12 R93 R94 R95 R96 R97 R98 R100 R101	R101 R20 R19 R18 R17 R15 R15 R14 R13 R12	R111 R36 R35 R34 R32 R31 R30 R29
	Pag	ge_0	20		Pag	ge_C	:1		Pag	pe_C	31		R109 R110 R111 R112 R113 R114 R115 R116 R117	R12 R93 R94 R95 R96 R97 R98 R99 R100 R100 R100	R101 R20 R19 R18 R17 R15 R14 R13 R14 R13	R111 R36 R35 R34 R33 R31 R31 R30 R29 R28
	Pa	ge_C	:0		Pag	ge_C	at the state of th		Pag	ne_C	:31		R109 R110 R111 R1112 R113 R114 R115 R116 R117 R119	R93 R94 R95 R96 R97 R98 R99 R100 R101 R102 R103	R101  R20 R19 R18 R17 R16 R15 R14 R13 R14 R13	R111 R36 R35 R34 R33 R31 R30 R29 R27 R26
	Pa	ge_C	50		Pag	ge_C	at the state of th		Pag	ne_C	31		R109 R110 R111 R112 R113 R114 R115 R116 R117 R118 R119	R12 R93 R94 R95 R96 R97 R98 R100 R101 R102 R103 R104	R101 R20 R19 R18 R17 R15 R14 R13 R12 R11 R10 R9	R36 R36 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 R27
	Pa	ge_C	30		Pag	ge_C	at+		Pag	ge_C	31		R109 R110 R111 R112 R113 R115 R116 R117 R118 R119 R120 R121	R12 R93 R94 R95 R96 R97 R100 R101 R102 R103 R104 R105	R101 R20 R19 R16 R17 R16 R13 R12 R11 R10 R9	R111 R36 R38 R34 R31 R30 R29 R28 R27 R26 R25 R26
	Pa	ge_C	:0		Pag	ge_C	al ·		Pag	ge_C	31		R109 R110 R111 R112 R113 R114 R115 R116 R117 R118 R119 R120 R121 R122	R93 R94 R95 R96 R97 R98 R100 R100 R101 R102 R103 R104 R105 R106	R101 R20 R19 R18 R15 R15 R14 R15 R10 R9 R8	R311 R36 R36 R37 R31 R30 R29 R26 R27 R26 R27 R26 R27
	Pa	ge_C	:0		Pag	ge_C	ed ·		Pag	pe_C	31		R109 R110 R111 R1112 R113 R114 R115 R116 R117 R119 R120 R121 R121 R122 R123	R93 R94 R95 R96 R97 R98 R99 R100 R101 R102 R103 R104 R105 R106 R107	R101 R20 R19 R18 R15 R14 R13 R11 R10 R9 R8	R111 R36 R36 R37 R31 R30 R27 R26 R27 R26 R25 R23 R24
	Pa	ge_C	50		Pag	ge_C	at ·		Pag	pe_C	31		R109 R110 R111 R112 R113 R114 R115 R116 R117 R118 R119 R120 R121 R122 R123 R124	R12 R93 R94 R95 R96 R97 R98 R99 R100 R101 R102 R103 R104 R105 R106 R107 R108	R101 R20 R19 R18 R17 R15 R14 R13 R12 R11 R10 R9 R8 R7 R6 R5	R36 R36 R35 R34 R33 R32 R31 R30 R29 R28 R26 R25 R27 R27 R27 R27 R27 R27 R27 R27 R27 R27
	Pa	ge_C	50		Pag	ge_C	at ·		Pag	ge_C	31		R109 R110 R111 R111 R112 R113 R114 R115 R116 R117 R118 R119 R120 R121 R122 R123 R124 R125	R12 R93 R94 R95 R96 R97 R100 R100 R101 R102 R103 R104 R105 R106 R107 R108 R109	R101 R20 R19 R18 R15 R14 R13 R11 R10 R9 R8	R311 R36 R33 R34 R33 R32 R22 R22 R22 R22 R22 R22 R22 R22
	Pa	ge_C	:0		Pag	ge_C	at the state of th		Pag	je_C	31		R109 R110 R111 R111 R112 R113 R114 R115 R116 R119 R120 R121 R122 R123 R124 R125 R126	R93 R94 R95 R96 R97 R98 R100 R100 R101 R102 R103 R104 R105 R106 R107 R108 R109 R1109	R101 R20 R19 R18 R17 R15 R14 R13 R12 R11 R10 R9 R8 R7 R6 R5 R4	R311 R36 R35 R34 R33 R31 R36 R22 R27 R22 R22 R23 R22 R21 R21 R21 R31 R31 R31 R32 R31 R32 R31 R32 R32 R33 R33 R34 R35 R35 R35 R35 R35 R35 R35 R35 R35 R35
	Pa	ge_C	:0		Pag	ge_C	x1		Pag	e_C	31		R109 R110 R111 R1112 R113 R114 R115 R116 R117 R118 R119 R120 R121 R122 R123 R124 R125 R125 R127	R12 R93 R94 R95 R96 R97 R98 R99 R100 R101 R102 R103 R104 R105 R106 R107 R108 R109 R109 R110 R110	R101 R20 R19 R18 R15 R14 R15 R14 R10 R9 R8 R7 R6 R5 R5 R7	R311 R33 R33 R33 R32 R32 R22 R22 R22 R22 R22
	Pay	ge_C	0		Pag	ge_C			Pag	e_C	31		R109 R110 R111 R111 R112 R113 R114 R115 R116 R119 R120 R121 R122 R123 R124 R125 R126	R93 R94 R95 R96 R97 R98 R100 R100 R101 R102 R103 R104 R105 R106 R107 R108 R109 R1109	R101 R20 R19 R18 R15 R15 R14 R10 R9 R8 R7 R6 R8 R7 R6 R8	R311 R36 R33 R34 R33 R36 R22 R22 R22 R22 R22 R22 R22 R21 R21 R21
												82	R109 R110 R111 R1112 R113 R114 R115 R116 R117 R118 R119 R120 R121 R122 R123 R124 R125 R125 R127	R12 R93 R94 R95 R96 R97 R98 R99 R100 R101 R102 R103 R104 R105 R106 R107 R108 R109 R109 R110 R110	R101  R20 R19 R18 R17 R16 R17 R16 R17 R16 R17 R17 R10 R9 R8 R7 R6 R7 R6 R7 R11 R10 R9 R8	R311 R33 R33 R33 R33 R33 R32 R22 R22 R22 R22
D		ge_C	8	δ	Pag 중	ge_C	8	8	Pag C129	e_0	31	C128	R109 R110 R111 R1112 R113 R114 R115 R116 R117 R118 R119 R120 R121 R122 R123 R124 R125 R125 R127	R12 R93 R94 R95 R96 R97 R98 R99 R100 R101 R102 R103 R104 R105 R106 R107 R108 R109 R109 R110 R110	R101  R20 R19 R18 R17 R16 R17 R16 R17 R16 R17 R17 R10 R9 R8 R7 R6 R7 R6 R7 R11 R10 R9 R8	R311 R336 R337 R337 R337 R337 R227 R227 R227 R227
				C125 C4				21 08	125			C1 C128	R109 R110 R111 R1112 R113 R114 R115 R116 R117 R118 R119 R120 R121 R122 R123 R124 R125 R125 R127	R12 R93 R94 R95 R96 R97 R98 R99 R100 R101 R102 R103 R104 R105 R106 R107 R108 R109 R109 R110 R110	R101  R20 R19 R18 R17 R16 R17 R16 R17 R16 R17 R17 R10 R9 R8 R7 R6 R7 R6 R7 R11 R10 R9 R8	R311 R36 R33 R34 R33 R32 R22 R22 R22 R22 R22 R21 R21 R21 R21 R2

Example: when MX=0, MY=0, SL=0, the corresponding data in SRAM as the pixels shown is: Row1 Page\_C0 ⇒ 11100100b

#### Reset

System reset can be initialized by setting RSTB terminal at low level when turning power on, receiving instruction from MPU. When RSTB becomes low, following procedure is occurred.

- Display off
- Display start line register become set by 0.(Z-address 0)

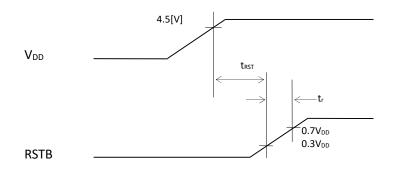
While RSTB is low level, no instruction except status read can be accepted. Reset status appears at DB4. After DB4 is low, any instruction can be accepted.

The Conditions of power supply at initial power up are shown in table 1.

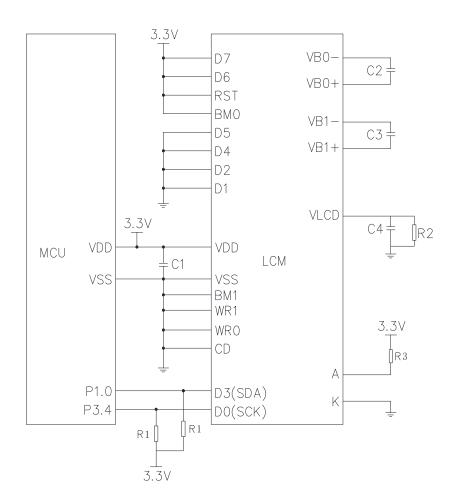


Table 1. Power Supply Initial Conditions

Item	Symbol	Min	Тур	Max	Unit
Reset time	tRST	1.0			ms
Rise time	tr			200	ns



# ■ POWER SUPPLY FOR LCM MODULE



#### I2C应用连接图

#### CON1:

1	VLCD	12	D5
2	VB0-	13	CD
3	VB1-	14	RST
4	ВМ1	15	D7
5	ВМО	16	D6
6	VB1+	17	D5
7	VB0+	18	D4
8	VDD	19	D3
9	VSS	20	D2
10	WR1	21	D1
11	WR0	22	D0

C1=C2=C3=2.2UF/25V C4=330nF/25V R1=10K R2=4.7M R3=10 ohm/0805



#### EXAMPLE

```
LCM
                 : GT128128D
         IC
;*
                 : UC1617s
        Data
                 : 2007.12.29 128x128dots 8 bit 8080 Mode -----Sunpring
#include<reg51.h>
#include<intrins.h>
sbit sck=P3<sup>7</sup>;
sbit sda=P1^0:
void init();
void font(int a);
void alldisplayon();
void displayoff();
void displaycom();
void displayseg();
void displaycom1();
void displayseg1();
void displaysnow();
void frame();
void delay(int t);
void write_com(unsigned char d);
void write come(unsigned char d);
void write data(unsigned char d);
void grayh();
void grayv();
void display_image1();
void init()
     delay(300);
     delay (300);
     delay(300);
write com(0xe2);//system rest
delay(300);
write com(0x25);//set temp -10^{\circ}+50°C
// write com(0x27);//set temp -20^{\circ}+70°C
write_com(0xd0);//set gray shade
write com(0xd4);//set gray shade
write com(0x2b);//panel loading
write com(0x2f);//set pump control
write com(0x81);//set vop 10.0v
write_com(OXC1);
```

```
write_com(0xc8);//
 write com(0x0B);
write_com(0x89);//set ram adders control
 write_com(0xa0);//set line rate
 write_com(0xc4);//set 1cd map control
 write\_com(0xe8);//1/6bias
 write com(0xf9);
 write_com(0xf1);//set com end 127
 write com(127);
write com(0xaD);//set disply enable BW-mode
 delay(300);
/* void display imagel (void)
int i;
//int j;
write_{com}(0x00);
write com(0x60);
write_{com}(0x70);
for (i=0; i<128*32; i++)
  write data(image1[i]);
   */
                           //全屏显示
void alldisplayon()
 int i, j;
 write_{com}(0x00);
 write\_com(0x60);
 write\_com(0x70);
 for (i=0; i<128; i++)
     for (j=0; j<32; j++)
        write_data(0xff);
void displayoff()
                      //清屏
     int i, j;
```

```
write\_com(0x00);
 write_com(0x60);
 write_{com}(0x70);
 for (i=0; i<128; i++)
     for (j=0; j<32; j++)
         write_data(0x00);
 }
void displaycom()
                       //横线
     int i, j;
 write_com(0x00);
 write\_com(0x60);
 write_com(0x70);
 for (i=0; i<64; i++)
     for (j=0; j<32; j++)
         write_data(0x00);
     for (j=0; j<32; j++)
         write_data(0xff);
                          //横线
void displaycom1()
     int i, j;
 write_{com}(0x00);
 write\_com(0x60);
 write_{com}(0x70);
 for (i=0; i<64; i++)
     for (j=0; j<32; j++)
         write_data(0xff);
     for(j=0;j<32;j++)
```

```
write_data(0x00);
     }
 }
                         //竖线
void displayseg()
{
     int i, j;
 write_{com}(0x00);
 write\_com(0x60);
 write_{com}(0x70);
 for (i=0; i<128; i++)
     for (j=0; j<32; j++)
         write_data(0xcc);
 }
                          //竖线
void displayseg1()
     int i, j;
 write\_com(0x00);
 write\_com(0x60);
 write_{com}(0x70);
 for (i=0; i<128; i++)
     for (j=0; j<32; j++)
         write_data(0x33);
 }
void displaysnow()
                           //雪花画面
     int i, j;
 write\_com(0x00);
 write_com(0x60);
 write_com(0x70);
 for (i=0; i<64; i++)
     for (j=0; j<32; j++)
```

```
write data(0xcc);
     for (j=0; j<32; j++)
        write_data(0x33);
 }
void iic_start(unsigned char cd)
                                            //lsend IIC start condition
 sda=1;
 _nop_( );
 _nop_();
 _nop_( );
 sck=1;
 _nop_();
 _nop_( );
 _nop_( );
 _nop_();
 _nop_();
 sda=0;
   _nop_();
 _nop_( );
 _nop_( );
 _nop_( );
 _nop_( );
 sck=0;
 _nop_( );
 _nop_();
 sda=0;
 _nop_( );
 _nop_( );
 sck=1;
 _nop_();
 _nop_( );
 sck=0;
 _nop_();
 _nop_( );
 sda=1;
 _nop_();
```

```
_nop_( );
sck=1;
_nop_( );
_nop_();
sck=0;
_nop_( );
_nop_();
sda=1;
_nop_();
_nop_();
sck=1;
_nop_();
_nop_( );
sck=0;
_nop_( );
_nop_( );
sda=1;
_nop_();
_nop_();
sck=1;
_nop_( );
_nop_();
sck=0;//--
                    -sequence header(0111B)
_nop_( );
_nop_( );
sda=1;
_nop_( );
_nop_( );
sck=1;
_nop_( );
_nop_();
sck=0;
_nop_( );
_nop_();
sda=0;
_nop_( );
_nop_();
sck=1;
_nop_();
```

# **Tailorpixels**

```
_nop_();
          //----device address [1,0]
 sck=0;
 _nop_();
 _nop_();
   sda=cd;//cd=0(control); cd=1(data)
    _nop_();
 _nop_();
 sck=1;
 _nop_( );
 _nop_();
 sck=0;//--
          ----cd control
 _nop_( );
 _nop_();
 sda=0;//write mode(1 read mode)
 nop_();
 _nop_( );
 sck=1;
 _nop_();
 nop ();
 sck=0;//----
                  ----cd control
 _nop_();
 _nop_();
}
//-----write_iic {cd=0 (control); cd=1 (data)}-----//
void iic send(unsigned char y)
 unsigned char i;
             //---signal A----//
  sck=1;
    _nop_();
    _nop_();
    sck=0;
    _nop_();
    nop ();
 for (i=0; i<8; i++)
    sda=y\&0x80;
      sck=1;
      // _nop_( );
      // _nop_( );
```

```
// _nop_( );
     // _nop_();
         _nop_();
    /*if(y\&0x80)
        sda=1;
    else
        sda=0;
    sck=1;
       _nop_();
       _nop_( );
       _nop_();
       _nop_( );
       _nop_( );
    sck=0;
    //y=y<<1;*/
 // delay(1);
    sck=0;
    y < < =1;
 }
                //---signal A----//
    sck=1;
    _nop_();
    _nop_();
    sck=0;
    _nop_();
    _nop_();
}
/*===========
 I2c stop condition
 SDA low->high while SCL=high
 SCL
 SDA
void iic_stop()
{
       sda=0;
       _nop_();
       _nop_();
       _nop_();
       _nop_();
       sck=0;
```

```
_nop_();
        sck=1;
        _nop_();
        _nop_();
        _nop_();
        _nop_();
        _nop_();
        sda=1;
        _nop_();
        _nop_();
        _nop_();
        _nop_();
void write_com(unsigned char d)
     iic_start(0);
     iic_send(d);
     iic_stop();
void write_come(unsigned char d)
{
     iic_start(0);
     iic_send(d);
     iic_stop();
void write_data(unsigned char d)
{
     iic_start(1);
     iic_send(d);
     iic_stop();
void delay(int t)
 register int i, j;
 for (i=0; i < t; i++)
 for(j=0;j<125;j++);
```

```
void main()
while(1)
 {
 init();
 displayoff();
    delay(1000);
   alldisplayon();
   delay(1000);
 displayoff();
    delay(1000);
    displaycom();
    delay(1000);
//
      press();
 displayoff();
    delay(1000);
      displayoff();
    displaycom1();
    delay(1000);
 displayoff();
    delay(1000);
    displayseg();
    delay(1000);
//
      press();
      displayoff();
 displayoff();
    delay(1000);
    displaysegl();
    delay(1000);
//
      press();
//
      displayoff();
 displayoff();
    delay(1000);
    displaysnow();
    delay(1000);
      press();
```



# ■ RELIABILITY

# **▼** Content of Reliability Test

	Environmental Test												
No.	Test Item	Content of Test	Test Condition	Applicable Standard									
1	High temperature	Endurance test applying the high storage	80°C										
	storage	temperature for a long time.	200 hrs										
2	Low temperature	Endurance test applying the low storage	-30°C										
	storage	temperature for a long time.	200hrs										
3	High temperature	Endurance test applying the electric stress (Voltage & Current) and the thermal	50°C										
	operation	stress to the element for a long time.	200 hrs										
4	Low temperature	Endurance test applying the electric stress	-10 °C										
	operation	under low temperature for a long time.	200 hrs										
	High temperature/	Endurance test applying the high	50°C,	MIL-202E-103B									
5	Humidity storage	tempera-ture and high humidity storage	90 %RH	JIS-C5023									
	Training Storage	for a long time.	96 hrs	3.5 65625									
		Endurance test applying the electric stress	40°C										
6	High temperature /	(Voltage & Current) and temperature /	90 %RH	MIL-202E-103B									
	Humidity operation	humidity stress to the element for a long	96 hrs	JIS-C5023									
		time.	301113										
		Endurance test applying the low and high											
		temperature cycle. -10°C 25°C 50°C	-10°C/50°C										
7	Temperature cycle	30min. 25 C 30 C 30min.	10 cycles										
		1 cycle	,										
		Mechanical Test											
		TVICEI ai lieat	10~22Hz → 1.5mmp-p	MIL-202E-201A									
8	Vibration test	Endurance test applying the vibration during	$22\sim500\text{Hz}\rightarrow1.5\text{G}$	JIS-C5025									
	Vibration test	transportation and using.	Total 0.5hrs	JIS-C7022-A-10									
		Constructional and mechanical endurance	50G half sign	313 C7022 A 10									
9	Shock test	test applying the shock during	wave 11 msedc	MIL-202E-213B									
	SHOCK (CSC	transportation.	3 times of each direction	IVIIL ZOZL ZIJD									
	Atmospheric	Endurance test applying the atmospheric	115 mbar										
10	pressure test	pressure during transportation by air.	40 hrs	MIL-202E-105C									
	p. coo o toot	Others	1010										
			VS=800V , RS=1.5 kΩ										
11	Static electricity test	Endurance test applying the electric stress to	CS=100 pF	MIL-883B-3015.1									
	cade creationly test	the terminal.	1 time	MIIC-002D-2012.1									
<u></u>		l											

<sup>\*\*\*</sup> Supply voltage for logic system = 5V. Supply voltage for LCD system = Operating voltage at 25°C.

# **▼** Failure Judgement Criterion

Criterion Item		Test Item No.									Failure Judgment Criterion	
	1	2	3	4	5	6	7	8	9	10	11	
Basic specification												Out of the Basic Specification
Electrical characteristic												Out of the DC and AC Characteristic
Mechanical characteristic												Out of the Mechanical Specification Color change : Out of Limit Apperance Specification



Optical characteristic						Out of the Apperance Standard

#### ■ INSPECTION CRITERIA

see: IS-QC-001(液晶显示模块检验标准)

#### ■ PRECAUTIONS FOR USING LCD MODULES

### ▼ Handing Precautions

- (1) The display panel is made of glass. Do not subject it to a mechanical shock by dropping it or impact.
- (2) If the display panel is damaged and the liquid crystal substance leaks out, be sure not to get any in your mouth. If the substance contacts your skin or clothes, wash it off using soap and water.
- (3) Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- (4) The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.
- (5) If the display surface becomes contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten cloth with one of the following solvents:
  - Isopropyl alcohol
  - Ethyl alcohol
- (6) Solvents other than those above-mentioned may damage the polarizer. Especially, do not use the following.
  - Water
  - Ketone
  - Aromatic solvents
- (7) Exercise care to minimize corrosion of the electrode. Corrosion of the electrodes is accelerated by water droplets, moisture condensation or a current flow in a high-humidity environment.



### USING LCD MODULES

### Liquid Crystal Display Modules

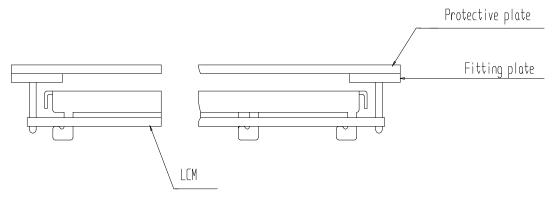
LCD is composed of glass and polarizer. Pay attention to the following items when handling.

- (1) Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peel-off may occur with high temperature and high humidity.
- (2) Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead (glass, tweezers, etc.).
- (3) N-hexane is recommended for cleaning the adhesives used to attach front/rear polarizers and reflectors made of organic substances which will be damaged by chemicals such as acetone, toluene, ethanol and isopropylalcohol.
- (4) When the display surface becomes dusty, wipe gently with absorbent cotton or other soft material like chamois soaked in petroleum benzin. Do not scrub hard to avoid damaging the display surface.
- (5) Wipe off saliva or water drops immediately, contact with water over a long period of time may cause deformation or color fading.
- (6) Avoid contacting oil and fats.
- (7) Condensation on the surface and contact with terminals due to cold will damage, stain or dirty the polarizers. After products are tested at low temperature they must be warmed up in a container before coming is contacting with room temperature air.
- (8) Do not put or attach anything on the display area to avoid leaving marks on.
- (9) Do not touch the display with bare hands. This will stain the display area and degradate insulation between terminals (some cosmetics are determinated to the polarizers).
- (10) As glass is fragile. It tends to become or chipped during handling especially on the edges. Please avoid dropping or jarring.

# Installing LCD Modules

The hole in the printed circuit board is used to fix LCM as shown in the picture below. Attend to the following items when installing the LCM.

(1) Cover the surface with a transparent protective plate to protect the polarizer and LC cell.



(2) When assembling the LCM into other equipment, the spacer to the bit between the LCM and the fitting plate should have enough height to avoid causing stress to the module surface, refer to the individual specifications for measurements. The measurement tolerance should be  $\pm 0.1$ mm.

# Precaution for Handing LCD Modules

Since LCM has been assembled and adjusted with a high degree of precision, avoid applying excessive shocks to the module or making any alterations or modifications to it.



- (1) Do not alter, modify or change the shape of the tab on the metal frame.
- (2) Do not make extra holes on the printed circuit board, modify its shape or change the positions of components to be attached.
- (3) Do not damage or modify the pattern writing on the printed circuit board.
- (4) Absolutely do not modify the zebra rubber strip (conductive rubber) or heat seal connector.
- (5) Except for soldering the interface, do not make any alterations or modifications with a soldering iron.
- (6) Do not drop, bend or twist LCM.

### **▼** Electro-Static Discharge Control

Since this module uses a CMOS LSI, the same careful attention should be paid to electrostatic discharge as for an ordinary CMOS IC.

- (1) Make certain that you are grounded when handing LCM.
- (2) Before remove LCM from its packing case or incorporating it into a set, be sure the module and your body have the same electric potential.
- (3) When soldering the terminal of LCM, make certain the AC power source for the soldering iron does not leak.
- (4) When using an electric screwdriver to attach LCM, the screwdriver should be of ground potentiality to minimize as much as possible any transmission of electromagnetic waves produced sparks coming from the commutator of the motor.
- (5) As far as possible make the electric potential of your work clothes and that of the work bench the ground potential.
- (6) To reduce the generation of static electricity be careful that the air in the work is not too dried. A relative humidity of 50%-60% is recommended.

### Precaution for soldering to the LCM

- (1) Observe the following when soldering lead wire, connector cable and etc. to the LCM.
  - Soldering iron temperature : 280°C  $\pm$  10°C.
  - Soldering time: 3-4 sec.
  - Solder: eutectic solder.

If soldering flux is used, be sure to remove any remaining flux after finishing to soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended that you protect the LCD surface with a cover during soldering to prevent any damage dur to flux spatters.

- (2) When soldering the electroluminescent panel and PC board, the panel and board should not be detached more than three times. This maximum number is determined by the temperature and time conditions mentioned above, though there may be some variance depending on the temperature of the soldering iron.
- (3) When remove the electroluminescent panel from the PC board, be sure the solder has completely melted, the soldered pad on the PC board could be damaged.

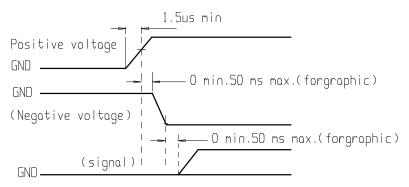
# Precautions for Operation

- (1) Viewing angle varies with the change of liquid crystal driving voltage (VO). Adjust VO to show the best contrast.
- (2) Driving the LCD in the voltage above the limit shortens its life.
- (3) Response time is greatly delayed at temperature below the operating temperature range. However, this does not mean the LCD will be out of the order. It will recover when it returns to the specified temperature range.
- (4) If the display area is pushed hard during operation, the display will become abnormal. However, it will return to normal if it is turned off and then back on.
- (5) Condensation on terminals can cause an electrochemical reaction disrupting the terminal circuit.



Therefore, it must be used under the relative condition of 40°C, 50% RH.

(6) When turning the power on, input each signal after the positive/negative voltage becomes stable.



### Storage

When storing LCD's as spares for some years, the following precaution are necessary.

- (1) Store them in a sealed polyethylene bag. If properly sealed, there is no need for dessicant.
- (2) Store them in a dark place. Do not expose to sunlight or fluorescent light, keep the temperature between 0°C and 35°C.
- (3) The polarizer surface should not come in contact with any other objects. (We advise you to store them in the container in which they were shipped.)
- (4) Environmental conditions:
  - Do not leave them for more than 168hrs. at 80°C.
  - Should not be left for more than 48hrs. at -30°C.

### Safety

- (1) It is recommended to crush damaged or unnecessary LCD's into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.
- (2) If any liquid out of a damaged glass cell and comes in contact with the hands, wash off thoroughly with soap and water.

# Limited Warranty

Unless agreed between TPS and customer, TPS will replace or repair any of its LCD modules which are found to be functionally defective when inspected in accordance with TPS LCD acceptance standards (copies available upon request) for a period of one year from date of shipments. Cosmetic/visual defects must be returned to TPS within 90 days of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of TPS limited to repair and/or replacement on the terms set forth above. TPS will not be responsible for any subsequent or consequential events.

# Return LCM under warranty

No warranty can be granted if the precautions stated above have been disregarded. The typical examples of violations are :

- Broken LCD glass.
- PCB eyelet's damaged or modified.
- PCB conductors damaged.
- Circuit modified in any way, including addition of components.
- PCB tampered with by grinding, engraving or painting varnish.
- soldering to or modifying the bezel in any manner.

Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects. Any connectors or cable installed by the customer must be removed completely without damaging the PCB eyelet's, conductors and terminals.